Title	Page	Title	Page	Title	Page
COVER PAGE	1	Sequence (RSVD) (DS3/S0ix)	41	GDDR6_VRAM1,2	81
BLACK DIAGRAM	2	042_INT IO (RSVD)	42	GDDR6_VRAM POWER	82
CPU (THML/JTAG)	3	INT IO (DC IN/BAT CON)	43	VRAM 5,6 (2/4)	83
CPU (DDI/EDP/TBT/TPC/)	4	Power (RSVD)	44	VRAM 7,8 (2/4)	84
CPU_DDR_CHA/CHB	5	POWER (RT6575D_5V/3D3V_S5)	45	RT8816_VGACORE	85
CPU_(CFG/IST)	6	POWER (RT3613EE_VCORE(1/2))	46	RT8237C_VRAM;RT5797_1D8V;RT5798_1D0V	86
CPU (VCCIN/VID)	7	POWER (RT3613EE_VCORE(2/2))	47	(RSVD)	87
CPU (VDDQ/VCC/VCCST)	8	Power (RSVD)	48	(RSVD)	88
CPU (RSVD)	9	Power (RSVD)	49	SCREW HOLE/EMI CAP	89
CPU (CORE Power Cap1)	10	POWER (RT6543_VCCAUX)	50	RF cap	90
CPU (Power Cap2)	11	POWER (RT8231_VDDQ/5934VPP)	51	(RSVD)	91
DDR (DDR4_CHA_DIMM1)	12	POWER (RSVD)	52	(RSVD)	92
DDR (DDR4_CHB_DIMM2)	13	POWER (RT8237C_1D8V)	53	(RSVD)	93
DDR (RSVD)	14	POWER (VNN/1D05V/12V)	54	(RSVD)	94
CPU_STRAP	15	Display_(RTD2136/Scalar)	55	(RSVD)	95
CPU (PCIE/SATA/USB)	16	Display_(RSVD_)	56	(RSVD)	96
CPU (PMU)	17	HDMI OUT	57	(RSVD)	97
CPU (SPI/LPC/SMBS/XTAL/CLK)	18	HDMI IN	58	(RSVD)	98
CPU (HAD/I2S/SD/DMIC)	19	Display (Backlight PW)	59	(Debug XDP)	99
CPU (UART/I2C/ISH)	20	INT IO (HDD)	60	TABLE OF CONTENT	100
CPU (CSI/EMMC/CNVi)	21	INT IO (NGFF Key-E WLAN)	61	CHANGE HISTORY	101
CPU (PCH-LP PWR&Caps)	22	INT IO (RSVD)	62	POWER SEQUENCING	102
	23	INT IO (SSD-NGFFM1)	63	POWER BLOCK DIAGRAM	103
CPU (VSS) CPU_RSVD/CFG	24	PWR BTN/SIDE KEY/LED	64	SMBUS BLOCK DIAGRAM	104
ECIO (IT8637	25	(RSVD)	65	THERMAL/AUDIO BLOCK DIAGRAM	105
Flash/RTC	26	(RSVD)	66	(Debug XDP)	106
AUDIO_ALC255/ALC256	27	(RSVD)	67		
Audio (Audio AMP)	28	Debug (Debug connector)	68		
Audio (Speaker/HPMIC)	29	(RSVD)	69		
Audio (Webcam/DMIC)	30	(RSVD)	70		
LAN_RTL8111H	31	Thunderbolt_BURNSIDE-BRIDGE(1/3)	71		
RJ45+TRANSFORMER	32	(Thunderbolt(PD_PTPS65992D)(2/3)	72		
SD/CR_RTS5176	33	(Thunderbolt(3/3)/Type C Conn)	73		
USB (USB2.0 CON)	34	(RSVD)	74		
USB (USB3.0 GEN1/GEN2)	35	(RSVD)	75		
USB (USB Charger)	36	GPU(1/5) PEG	76		
USB (Touch)	37	GPU(2/5)DIGITALOUT	77		
USB (USB3.0 Redriver)	38	GPU(3/5):VRAM I/F	78		
Sequence (RSVD)	39	GPU(4/5):GPIO/STRAP	79		
POWER SEQUENCING	40	GPU(5/5):PWR/GND	80		

Delphi 215i & 238i Schematic Document

BOM Configuration
(R_):Unmount
(O_):OCP
(DBG_):Debug
(T_):Touch function
(TBT_):Thunderbolt
(NONTBT_): Non Thunderbolt
(AMP_): Scallar+AMP
(NONAMP_):RTD2136
(G_):NV GPU N18S
(U_): UMA
(ALC256_):Audio ALC256
(ALC255_):Audio ALC255
(15W_): Vcore 2phase
(28W_): Vcore 3phase
(215I_): 215I MB
(238I_): 238I MB
(M_): GPU RAM MICRON
(S_): GPU RAM SAMSUNG

Project code : 3PD0EE01A001 (215i)
3PD0EE010001 (238i)
PCB No : 19476/19478 (215i/238i)
Revision : 1A
Project Name : Delphi 215i & 238i
Size : 204mm x145.3mm (215i)
264mm x 145.3mm (238i)

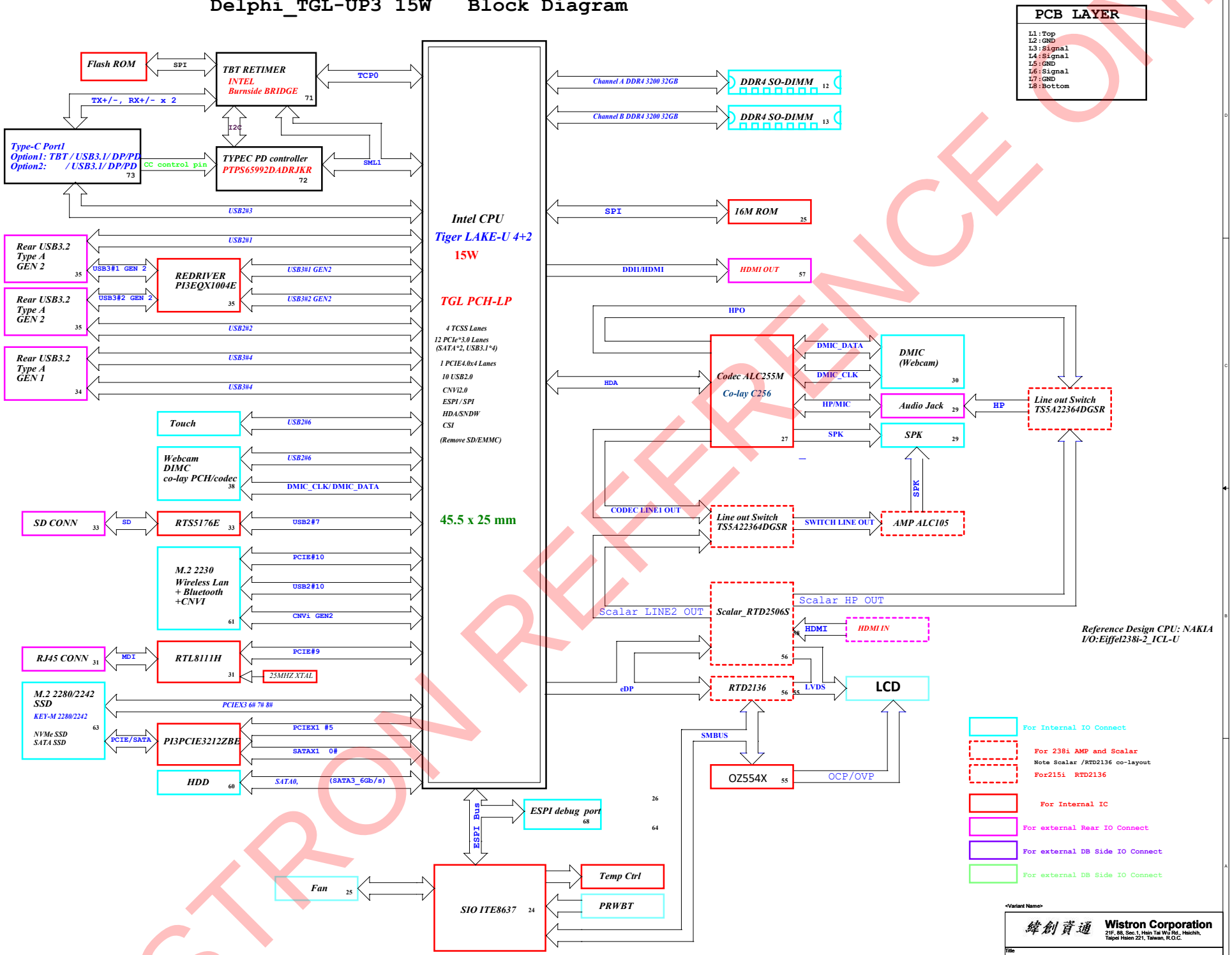
WISTRON REFERENCE ONLY

<Core Design>

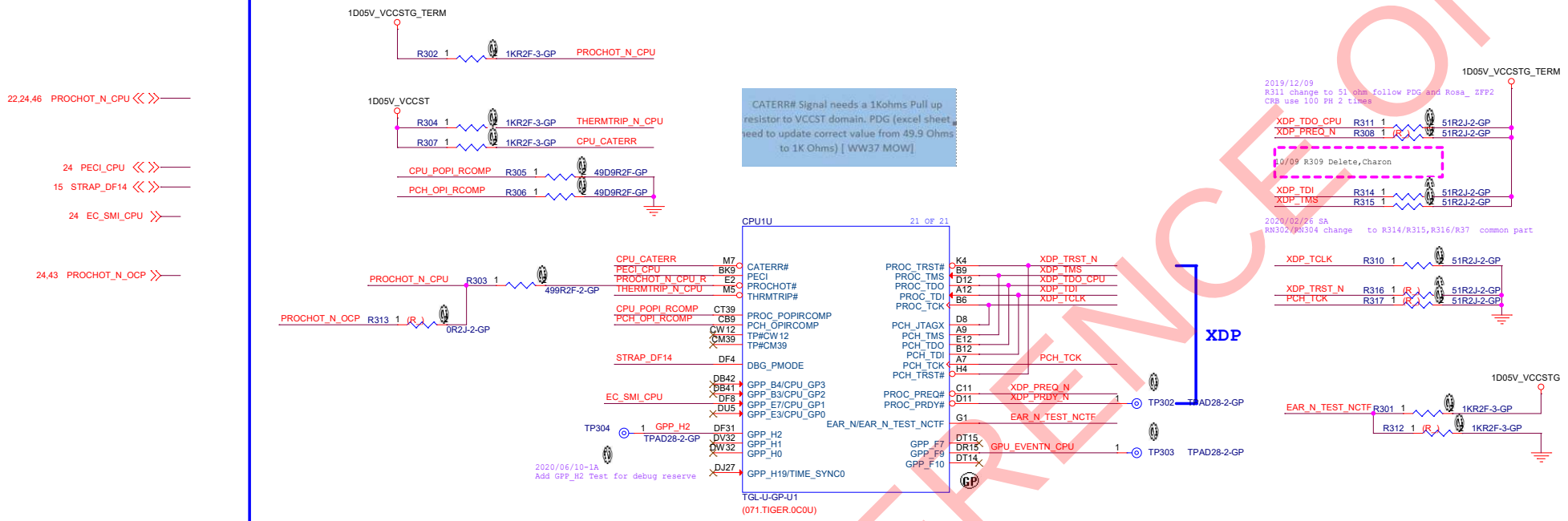
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page
Size: C | Document Number: Delphi_TGL-U | Rev: -1
Date: Wednesday, September 16, 2020 | Sheet 1 of 106

Delphi_TGL-UP3 15W Block Diagram



WISTRON REFERENCE ONLY



Signal	Usage	When Sampled	Comment
GPP_F7	Reserved	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F10	Reserved	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

<Variant Name>

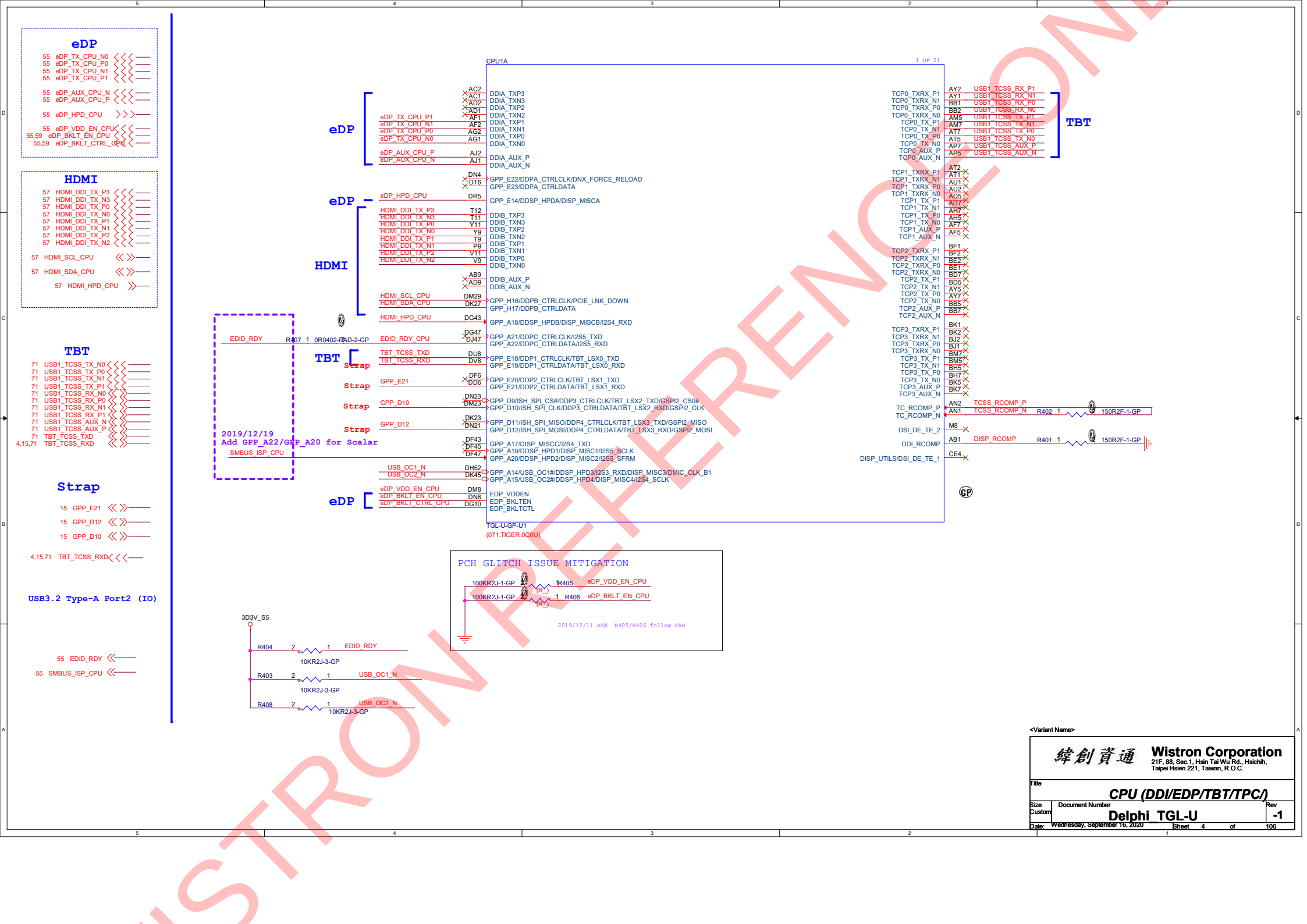
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (THML/JTAG)

Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 3 of 106

WISTRON REFERENCE ONLY



WISTRON REFERENCE ONLY

<Variant Name>

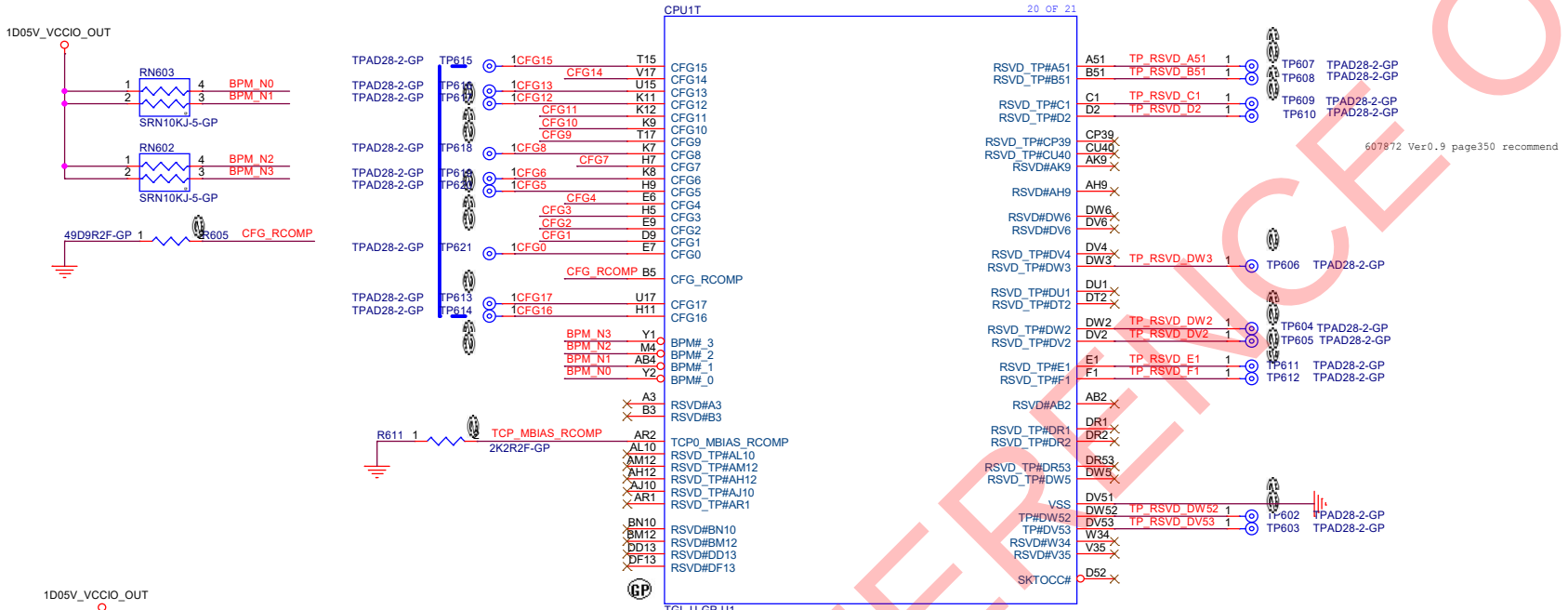
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

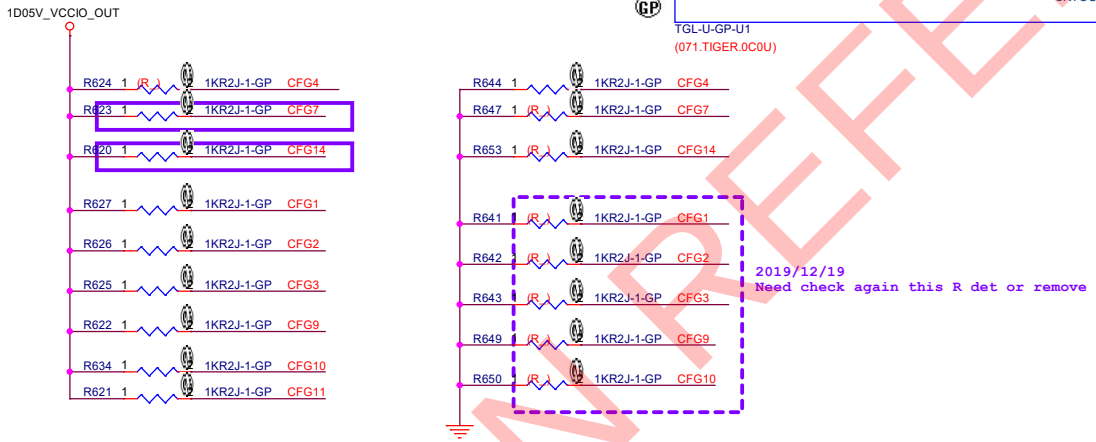
Title: CPU (DDI/EDP/TBT/TPC/)

Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 4 of 106

WISTRON REFERENCE ONLY





CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: (DEFAULT)NORMAL OPERATION;
	0: LANE REVERSAL

DISPLAY PORT PRESENCE STRAP	
CFG4	0: ENABLED
	AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1: DISABLED
	NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

PCIE PORT BIFURCATION STRAPS	
CFG[6:5]	11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
	10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
	01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
	00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

<Core Design>

緯創資通 Wistron Corporation
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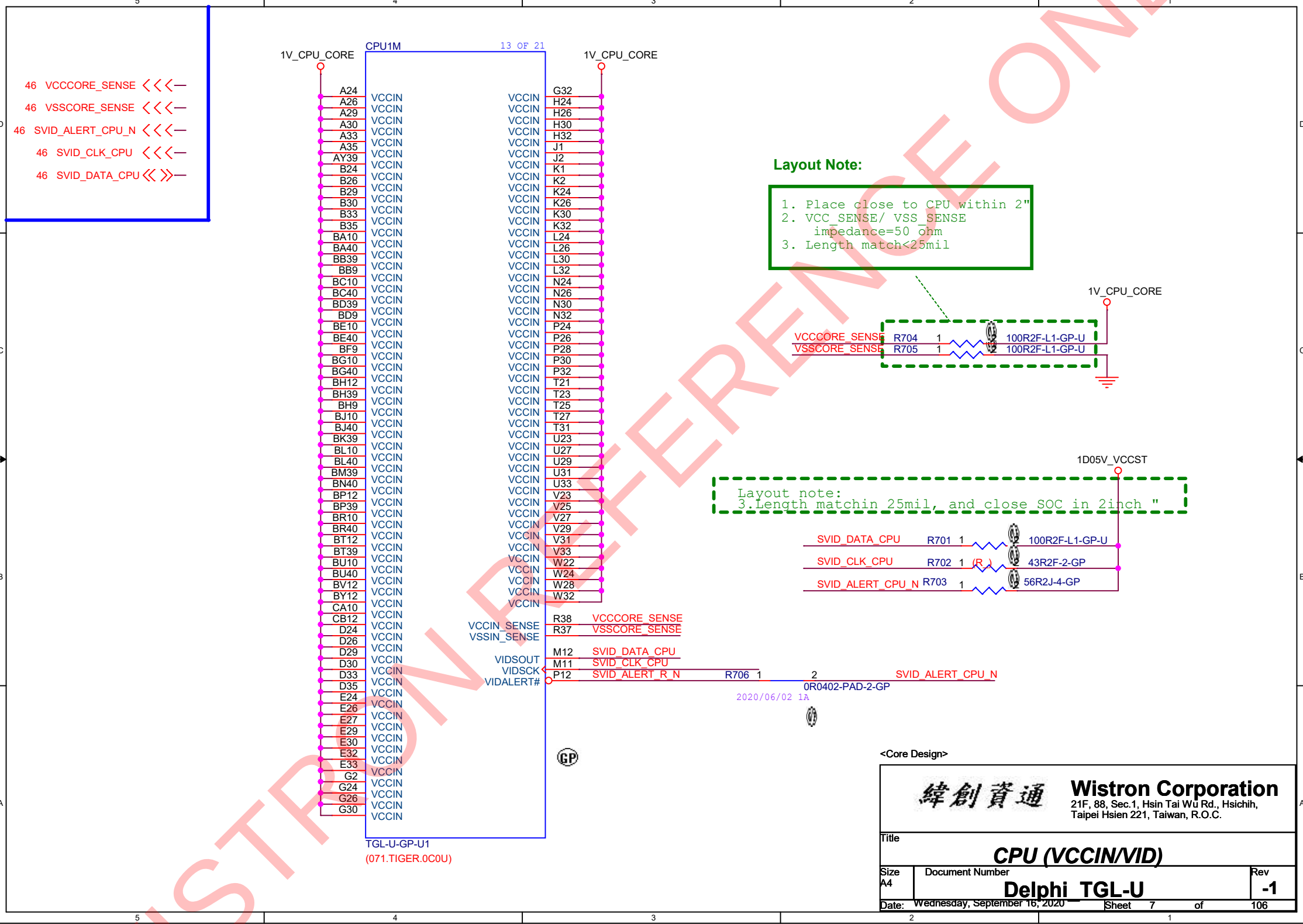
Title: CPU (CFG/IST)

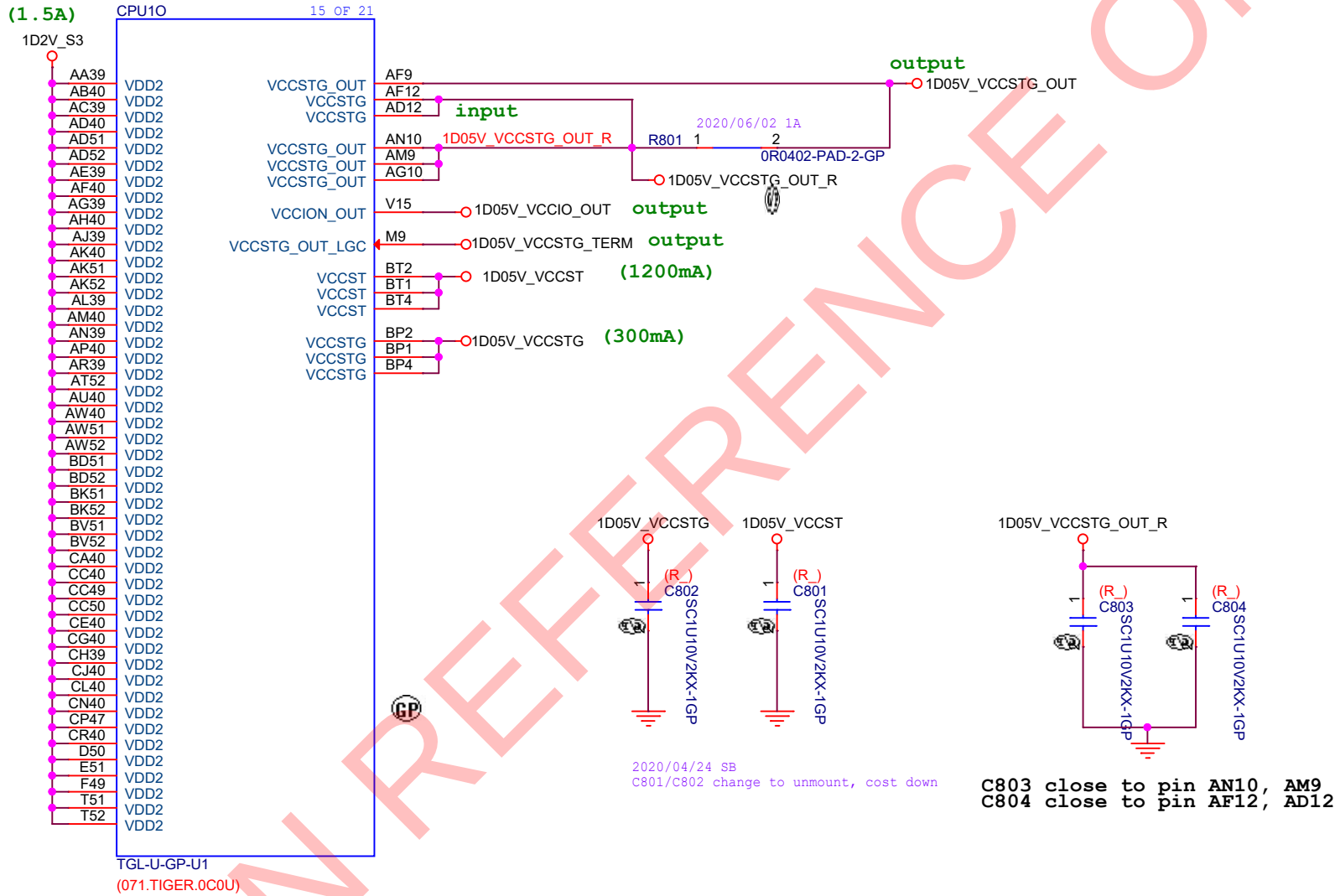
Size	Document Number	Rev
A3	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 6 of 106

WISTRON PREFERENCE ONLY



WISTRON REFERENCE ONLY



Lack of VCCPLL_OC / VCC1P8A / VCCPLL

WISTRON REFERENCE ONLY

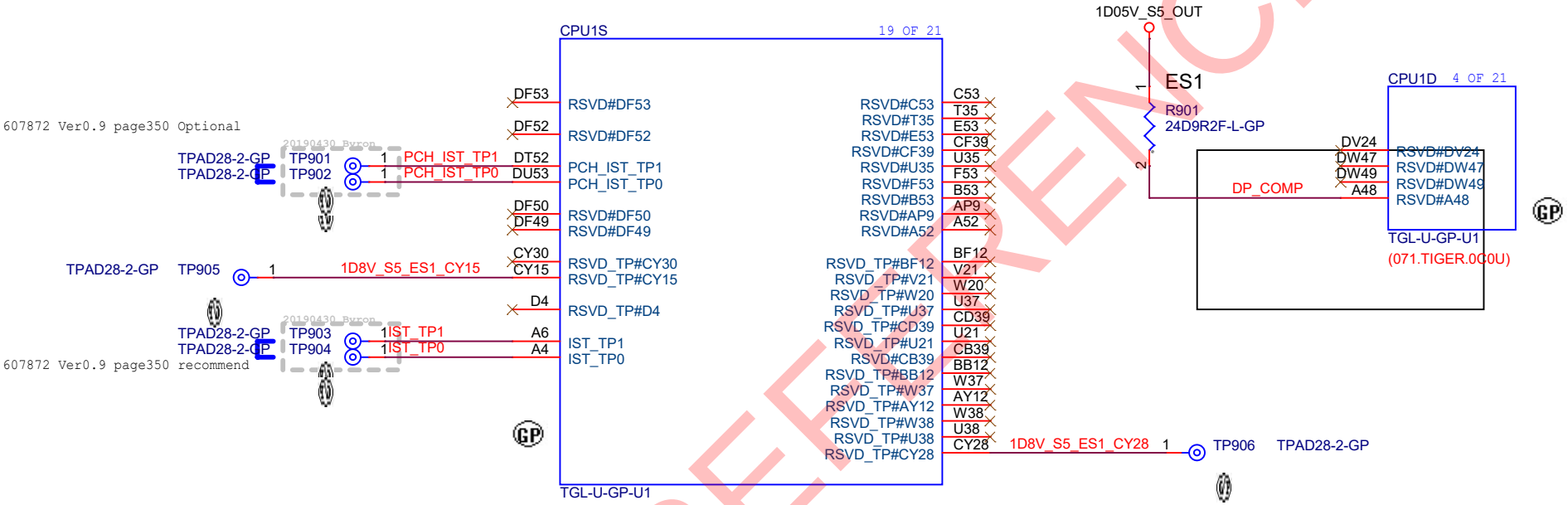
<Core Design>

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VDDQ/VCC/VCCST)

Size	Document Number	Rev
A4	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 8 of 106



WISTRON REFERENCE ONLY

<Core Design>

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RSVD)

Size	Document Number	Rev
A4	Delphi_TGL-U	-1

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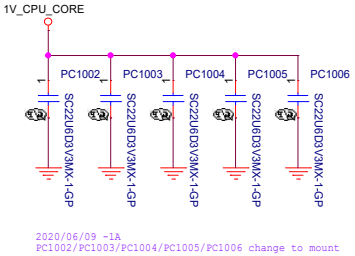
Main Func = CPU

1V_CPU_CORE

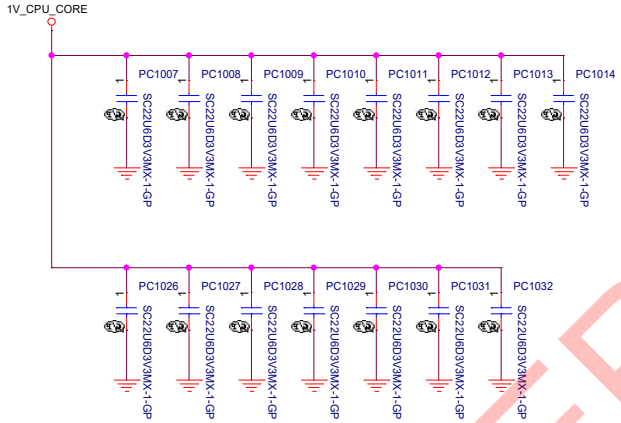
ICL_U42/TGL_U42_28W

U42
IccMax current-10ms max = 70 A

22uF	PCS	Cap
U42	15	330uF*1



2020/06/09 -1A
PC1002/PC1003/PC1004/PC1005/PC1006 change to mount



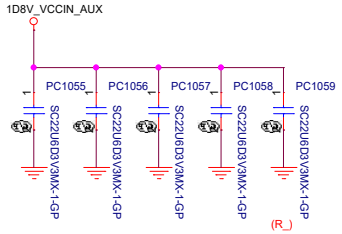
*10uF *6pcs*

2020/02/19
del cap C1001/C1002/C1003/C1004/C1005/C1006
1V_CPU_CORE 10uF *6pcs

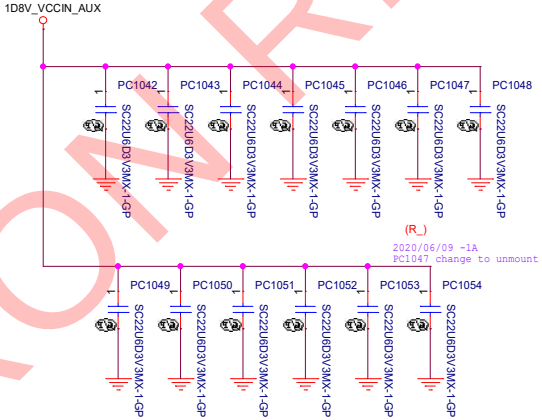
1D8V_VCCIN_AUX

RT6543A

22uF	PCS	Cap
U42	13	330uF*1



2020/06/09 -1A
PC1055/PC1056/PC1057/PC1058 change to mount



2020/06/09 -1A
PC1047 change to unmount

*10uF *4pcs*

2020/02/19
del cap C1007/C1008/C1009/C1010
1D8V_VCCIN_AUX 10uF *4pcs

WISTRON REFERENCE ONLY

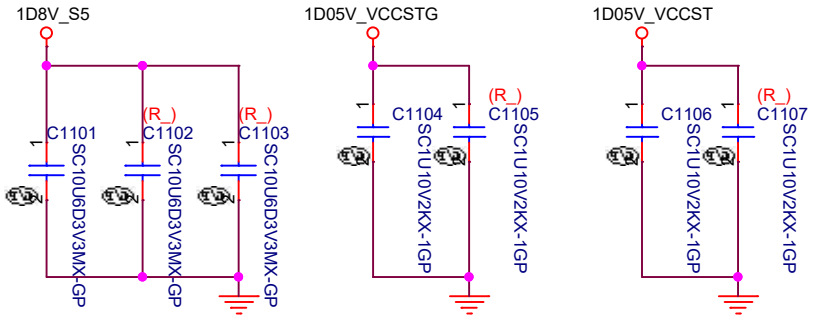
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

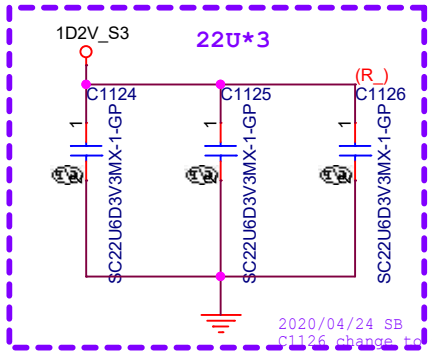
Title: CPU (CORE Power Cap1)

Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 10 of 106

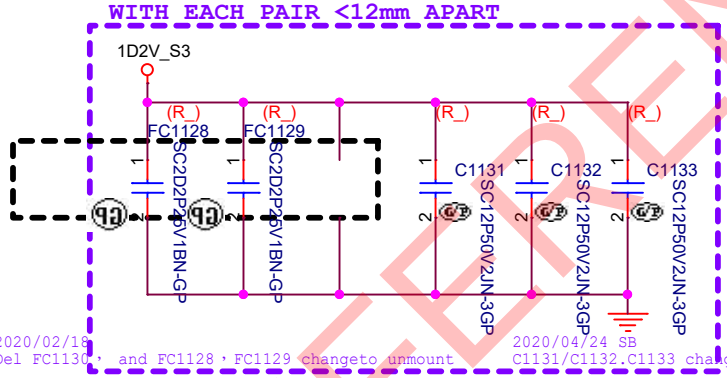


PLACE on CPU Same Side



2020/04/24 SB
C1126 change to unmount

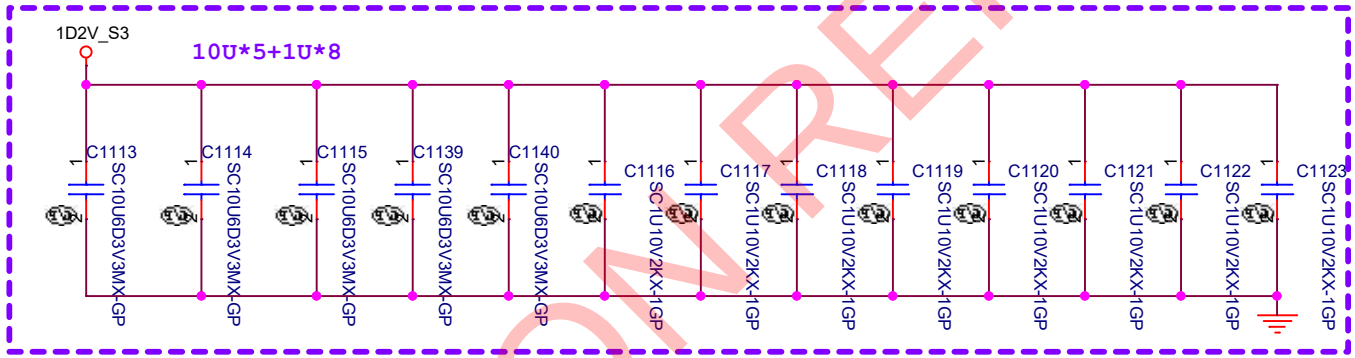
EMC CAPS - PLACE <4mm FROM SOC VDDQ, WITH EACH PAIR <12mm APART



2020/02/18
Del FC1130, and FC1128, FC1129 changeto unmount

2020/04/24 SB
C1131/C1132.C1133 changeto unmount

PLACE on BACK SIDE



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (Power Cap2)***

Size	Document Number	Rev
A4	Delphi_TGL-U	-1

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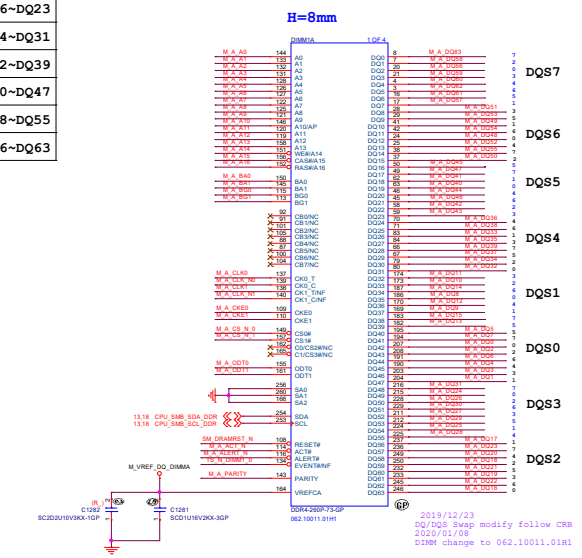
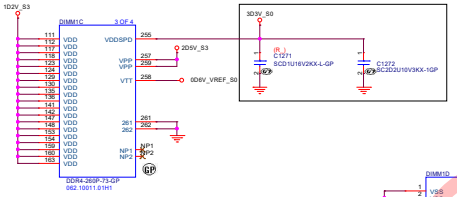
WISTRON REFERENCE ONLY

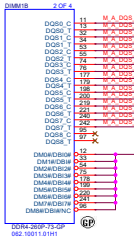
SSID = DDR4 CHA

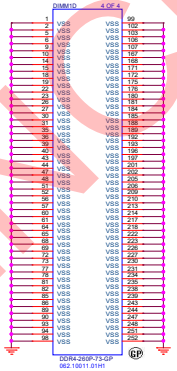
Please notice that signal BG1 (pin:M9) and UZQ (pin:E9) are required

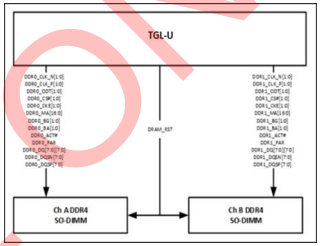
DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

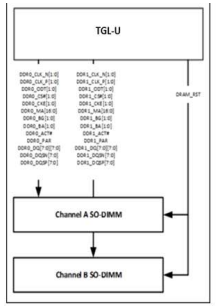


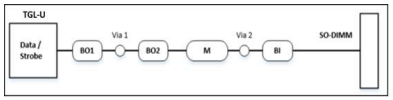


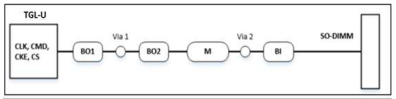


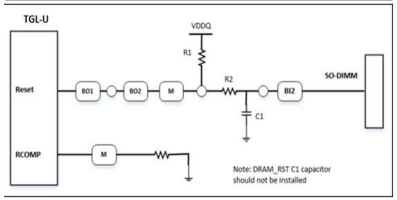


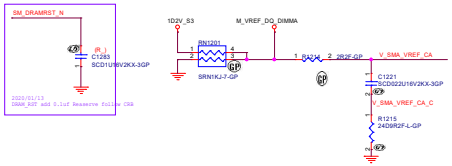


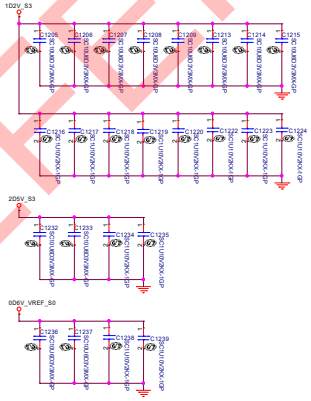












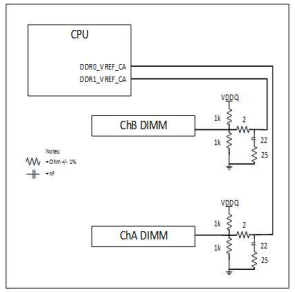


Table 4-31. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to DIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	1 cap per DIMM. Place close to DIMM	2x 0.1µF (0402)
		1 cap per DIMM. Place close to DIMM	2x 2.2µF (0402)

Note:
1. Total quantity is referring to 2 channels.

INTEL CONFIDENTIAL
INTEL REFERENCE ONLY

SSID = DDR4 CHB

Note:
SO-DIMMB SPD Address is 0xA4

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

SPD Address of DIMM1

SPD SA1	1
SPD SA0	0

H=4mm

DIMM2A 1 OF 4

DDR4-260P-65-GP
062.10011.01C1

DQS5 DQS4 DQS7 DQS6 DQS1 DQS0 DQS3 DQS2

2019/12/23
DQ/DQS Swap modify follow CRB
2020/01/08
DIMM change to 062.10011.01H1

DIMM2C 3 OF 4

DDR4-260P-65-GP
062.10011.01C1

need close to PIN 255

DIMM2B 2 OF 4

DDR4-260P-65-GP
062.10011.01C1

DIMM2D 4 OF 4

DDR4-260P-65-GP
062.10011.01C1

Place these Caps near DIMM1.

Thermal EVENT

Table 4-31. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to DIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	1 cap per DIMM. Place close to DIMM	2x 0.1µF (0402)
		1 cap per DIMM. Place close to DIMM	2x 2.2µF (0402)

Note:
1. Total quantity is referring to 2 channels.

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Title: DDR (DDR4_CHB)

Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

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Title: ***DDR (RSVD)***

Size	Document Number	Rev
A	Delphi_TGL-U	-1

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18,25 SPI_SI_ROM
18,25 SPI_WP_ROM
18,25 SPI_HOLD_ROM

21,61 CNV_RGI_DT
18 SML0_ALERT_N
18 GPP_E6
19 HDA_SDOUT_CPU
4,71 TBT_TCSS_RXD
4 GPP_D10
3 STRAP_DF14
4 GPP_D12
4 GPP_E21
18 GPP_E10
18 GPP_E11

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic	3D3V_S5 =20K PD= R1501 4K7R2J-2-GP SML0_ALERT_N R1502 20K5R2F-GP	3D3V_S5 =NO INTERNAL= R1503 100KR2J-1-GP SPI_SI_ROM BOOT_HALT Close to U2501 R1511 4K7R2J-2-GP	1D8V_S5 =NO INTERNAL= R1509 100KR2J-1-GP sky 0329 check if PH 3D3V_SUS ??? GPP_E6 R1512 4K7R2J-2-GP	=20K PD=	3D3V_S5 =NO INTERNAL= R1506 100KR2J-1-GP SPI_WP_ROM Close to U2501 R1514 4K7R2J-2-GP CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	=20K PD= * PH as VCCPGPPR 1D8V_GPPR_S5 R1509 4K7R2J-2-GP ME_UNLOCK R1515 0R0402-PAD-2-GP HDA_SDOUT_CPU 2020/06/02 1A	1D8V_S5 =NO INTERNAL= CRB use 47K Need check R1507 100KR2J-1-GP CNV_RGI_DT Close to M.2 R1516 4K7R2J-2-GP
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0	DBG_PMODE	GPP_E10	GPP_E11
Schematic	E19 3D3V_S5 =NO INTERNAL= R1518 4K7R2J-2-GP TBT_TCSS_RXD R1521 20KR2J-L2-GP	E21 3D3V_S5 =NO INTERNAL= R1519 4K7R2J-2-GP GPP_E21 R1522 20KR2J-L2-GP	D10 3D3V_S5 =NO INTERNAL= R1520 4K7R2J-2-GP GPP_D10 R1523 20KR2J-L2-GP	D12 3D3V_S5 =NO INTERNAL= R1524 4K7R2J-2-GP GPP_D12 R1525 20KR2J-L2-GP	3D3V_S5 =NO INTERNAL= 2020/01/13 CRB use 100K NAKIA use4.7k R1526 100KR2J-1-GP SPI_HOLD_ROM Close to U2501 R1527 100KR2J-1-GP	1D05V_S5_OUT =20K PU= R1528 1KR2F-3-GP STRAP_DF14 R1529 1KR2F-3-GP	1D8V_S5 R1531 20KR2J-L2-GP GPP_E10	1D8V_S5 R1530 20KR2J-L2-GP GPP_E11
High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)		
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED		

Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**A0**	**GPP_E10**	**GPP_E11**		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	RA RB	RA RB		

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Title: CPU (STRAP)
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M.2 SSD

63 SSD_PCIE_TX_P0
63 SSD_PCIE_TX_N0
63 SSD_PCIE_RX_P0
63 SSD_PCIE_RX_N0

63 SSD_PCIE_TX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_RX_N1

63 SSD_PCIE_TX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_RX_P2
63 SSD_PCIE_RX_N2

63 SSD_PCIE_TX_P3
63 SSD_PCIE_TX_N3
63 SSD_PCIE_RX_P3
63 SSD_PCIE_RX_N3

63 M2_PEDET1
63 M2_DEVSLP1

GPU

LAN

31 LAN_PCIE_TX_N
31 LAN_PCIE_TX_P

31 LAN_PCIE_RX_N
31 LAN_PCIE_RX_P

WLAN

61 WLAN_PCIE_TX_N
61 WLAN_PCIE_TX_P

61 WLAN_PCIE_RX_N
61 WLAN_PCIE_RX_P

SATA

60 HDD_SATA_TX_P
60 HDD_SATA_TX_N
60 HDD_SATA_RX_P
60 HDD_SATA_RX_N

63 SSD_SATA_TX_P
63 SSD_SATA_TX_N
63 SSD_SATA_RX_P
63 SSD_SATA_RX_N

USB1

38 USB1_USB31_TX_P
38 USB1_USB31_TX_N
38 USB1_USB31_RX_P
38 USB1_USB31_RX_N

35 USB1_USB20_P
35 USB1_USB20_N

USB2

38 USB2_USB31_TX_P
38 USB2_USB31_TX_N
38 USB2_USB31_RX_P
38 USB2_USB31_RX_N

35 USB2_USB20_P
35 USB2_USB20_N

USB3

73 USB3_USB20_P
73 USB3_USB20_N

USB4

35 USB4_USB31_TX_P
35 USB4_USB31_TX_N
35 USB4_USB31_RX_P
35 USB4_USB31_RX_N

35 USB4_USB20_P
35 USB4_USB20_N

TOUCH

37 TS_USB20_N
37 TS_USB20_P

Camera

30 CCD_USB20_P
30 CCD_USB20_N

Card Reader

33 CARD1_USB20_P
33 CARD1_USB20_N

BT

61 BT_USB20_P
61 BT_USB20_N

USB2.0 PORT

34 USB8_USB20_P
34 USB8_USB20_N

Other

71,72 TBT_FORCE_PWR
71 PCH_TBT_PERST_N

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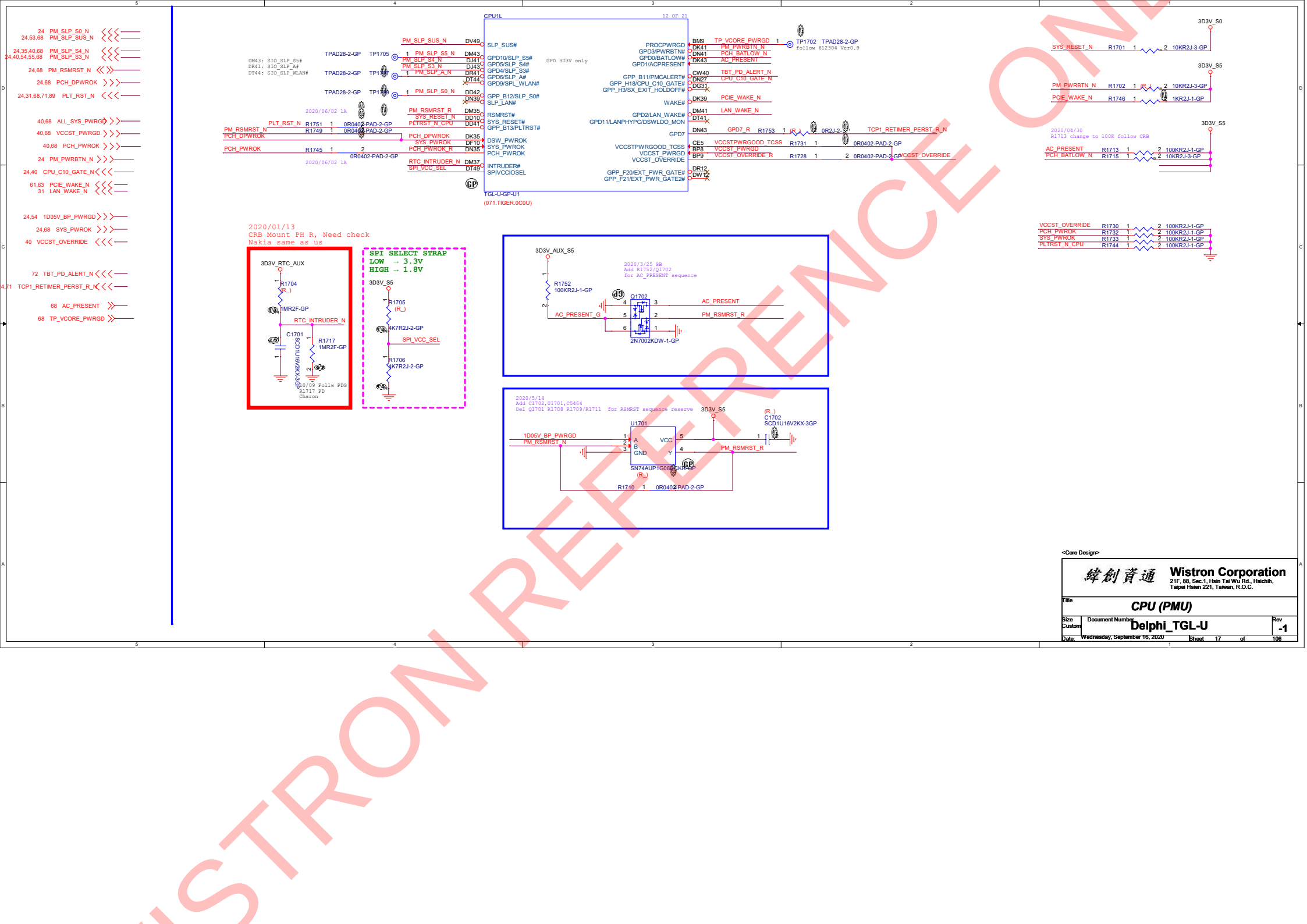

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SPI ROM

25 SPI_CLK_ROM
15,25 SPI_HOLD_ROM
15,25 SPI_WP_ROM
25 SPI_SO_ROM
15,25 SPI_SI_ROM
25 SPI_CS_ROM_N0

ESPI

24 ESPI_CPU_IO0
24 ESPI_CPU_IO1
24 ESPI_CPU_IO2
24 ESPI_CPU_IO3
24 ESPI_CPU_CS_N
24,68 ESPI_CPU_RST_EC_N
24 ESPI_CPU_CLK_EC
68 ESPI_CPU_CLK_DB

SMBUS

S5 smbus
55,61 CPU_SMB_SCL
55,61 CPU_SMB_SDA
S0 smbus
12,13 CPU_SMB_SDA_DDR
12,13 CPU_SMB_SCL_DDR
GPU
72 CPU_SMB_SCL_SML1
72 CPU_SMB_SDA_SML1
TBT PD
71 CPU_SMB_SCL_SML0
71 CPU_SMB_SDA_SML0

24 CPU_SMB_SCL_EC
24 CPU_SMB_SDA_EC

OTHER

24 RTCRST_ON
25,68 RTC_RST_N
64 KEY0_TEST
61,63,68 SUS_CLK_CPU

HW STRAP

15 SML0_ALERT_N
15 GPP_E6
15 GPP_E10
15 GPP_E11

PCIE CLK

LAN CLK
31 LAN_CLK_CPU_P
31 LAN_CLK_CPU_N
31 LAN_CLKREQ_CPU_N
WLAN CLK
61 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N
61 WLAN_CLKREQ_CPU_N
SSD CLK
63 SSD_CLK_CPU_N
63 SSD_CLK_CPU_P
63 SSD_CLKREQ_CPU_N
GPU CLK

68 SRTC_RST_N

DN19/SMBALERT#

TLS CONFIDENTIALITY
LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

CY50/SMBALERT#

CPUNSSC CLOCK FREQ
HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)
LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

Need check STRAP PH 是否需要再串阻 之前

2019/12/16 change to 75 ohm follow check list V1.0
2020//16 change to 62 ohm follow check list V1.1

CPU1E — 5 OF 21

SPI_CLK_ROM R1826 SPI_HOLD_ROM R1827 SPI_WP_ROM R1828 SPI_SO_ROM R1829 SPI_SI_ROM R1830 — 62R2F-GP
SPI_CS_ROM_N0 R1837 0R0402-PAD-2-GP

SPI0_CLK_R_CPU DJ37
SPI0_HOLD_R_CPU DG35
SPI0_WP_R_CPU DJ39
SPI0_SO_R_CPU DJ33
SPI0_SI_R_CPU DJ35
SPI_CS_CPU_N0 DG37

SPI0_CLK
SPI0_IO3 Strap
SPI0_IO2 Strap
SPI0_MISO
SPI0_MOSI Strap
SPI0_CS1#
SPI0_CS0#
SPI0_CS2#

KEY0_TEST R1836 0R0402-PAD-2-GP — KEY0_TEST_CPU DJ6
2019/12/19 add GPIO E1 for Panel

GPP_E11 — DN5
GPP_E10 — DR6
DK6
DGPU_HOLD_RST_N — DV11
GPP_E6 — DW9
GC6_FB_EN — DT5
TPAD28-2-GP TP1801 — DN15

GPP_E11/SPI1_CLK/THC0_SPI1_CLK Strap
GPP_E2/SPI1_IO3/THC0_SPI1_IO3
GPP_E1/SPI1_IO2/THC0_SPI1_IO2
GPP_E12/SPI1_MISO_IO1/THC0_SPI1_IO1
GPP_E13/SPI1_MOSI_IO0/THC0_SPI1_IO0
GPP_E10/SPI1_CS#/THC0_SPI1_CS#
GPP_E8/SPI1_CS1#/SATA_LED#
GPP_E17/THC0_SPI1_INT#
GPP_E6/THC0_SPI1_RST#
GPP_F11/THC1_SPI2_CLK
GPP_F15/GSXSRESET#/THC1_SPI2_IO3
GPP_F14/GSXDIN/THC1_SPI2_IO2
GPP_F13/GSXSLOAD/THC1_SPI2_IO1
GPP_F12/GSXDOUT/THC1_SPI2_IO0
GPP_F16/GSXCLK/THC1_SPI2_CS#
GPP_F18/THC1_SPI2_INT#
GPP_F17/THC1_SPI2_RST#

DH3 CL_CLK
DH4 CL_DATA
DF2 CL_RST#

TGL-U-GP-U1
(071.TIGER.0C0U)

GPP_C0/SMBCLK — DK21 CPU_SMB_SCL
GPP_C1/SMBDATA — DM19 CPU_SMB_SDA
GPP_C2/SMBALERT# — DN19 CPU_SMB_ALERT_N
GPP_C3/SML0CLK — DM17 CPU_SMB_SCL_SML0
GPP_C4/SML0DATA — DN17 SML0_ALERT_N
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK — DK17 CPU_SMB_SCL_SML1
GPP_C7/SML1DATA — DJ17 CPU_SMB_SDA_SML1
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1# — CY50 SML1_ALERT_N

@S5 domain for TSMT1&WLAN&Scalar
@S0 domain for DIMM1&DIMM2
Strap Pin

TBT BB Strap Pin

DGPU TBT PD Strap Pin

GPP_A5/ESPI_CLK — DN53 ESPI_CPU_CLK_R — R1804 49D9R2F-GP — ESPI_CPU_CLK
GPP_A3/ESPI_IO3/SUSACK# — DJ53 ESPI_CPU_IO3_R — R1808 15R2F-2-GP — ESPI_CPU_IO3
GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK — DH50 ESPI_CPU_IO2_R — R1807 15R2F-2-GP — ESPI_CPU_IO2
GPP_A1/ESPI_IO1 — DP50 ESPI_CPU_IO1_R — R1806 15R2F-2-GP — ESPI_CPU_IO1
GPP_A0/ESPI_IO0 — DP52 ESPI_CPU_IO0_R — R1805 15R2F-2-GP — ESPI_CPU_IO0
GPP_A4/ESPI_CS# — DK52 ESPI_CPU_CS_N_R — R1809 2R0402-PAD-2-GP — ESPI_CPU_CS_N
GPP_A6/ESPI_RESET# — DL50 ESPI_CPU_RST_R_N — R1810 2R0402-PAD-2-GP — ESPI_CPU_RST_EC_N
R1814 75KR2J-GP

to EC,debug14pin

2020/06/02

ESPI_CPU_CLK R1832 0R0402-PAD-2-GP — ESPI_CPU_CLK_EC
R1833 0R2J-2-GP — ESPI_CPU_CLK_DB

11.08 3D3V_S0->3D3V_S5

3D3V_S5
CPU_SMB_SDA — RN1803 — CPU_SMB_SCL — SRN1KJ-7-GP
CPU_SMB_SCL_SML0 — RN1807 — CPU_SMB_SDA_SML0 — SRN1KJ-7-GP
CPU_SMB_SCL_SML1 — RN1801 — CPU_SMB_SDA_SML1 — SRN1KJ-7-GP
CPU_SMB_ALERT_N — R1823 4K7R2J-2-GP
DGPU_HOLD_RST_N — R1853 10KR2J-3-GP
2020/01/13 R1824/R1823/R1825 Change to 4.7k, Follow CRB NAKIA use 10k

1D8V_S5
CPU_SMB_ALERT_N — R1824 4K7R2J-2-GP
SML1_ALERT_N — R1825 4K7R2J-2-GP

2019/12/11 Add level shift for DDR SMBUS

3D3V_S0
RN1806 — CPU_SMB_SCL_DDR — CPU_SMB_SDA_DDR — SRN1KJ-7-GP
Q1801 2N7002KDW-1-GP
CPU_SMB_SCL — CPU_SMB_SCL_DDR
CPU_SMB_SDA — CPU_SMB_SDA_DDR

75.27002.F7C
2nd = 075.67002.007C
3rd = 075.27002.0E7C

CPU_SMB_SCL_SML0 — RN1808 — CPU_SMB_SDA_SML0 — SRN0J-6-GP — CPU_SMB_SCL_EC — CPU_SMB_SDA_EC
CPU_SMB_SCL_SML1 — RN1809 — CPU_SMB_SDA_SML1 — SRN0J-6-GP
2020/02/19 add SMBUS follow Nakia

CPU1K — 11 OF 21

M.2 SSD
LAN
WLAN
GPU

CLKOUT_PCIE_P6 BW1 / CLKOUT_PCIE_N6 BW2
CLKOUT_PCIE_P5 CB2 / CLKOUT_PCIE_N5 CB1
SSD_CLK_CPU_P — CLKOUT_PCIE_P4 BW4 / CLKOUT_PCIE_N4 BW5
LAN_CLK_CPU_P — CLKOUT_PCIE_P3 CL7 / CLKOUT_PCIE_N3 CL8
CLKOUT_PCIE_P2 CB4 / CLKOUT_PCIE_N2 CB5
WLAN_CLK_CPU_P — CLKOUT_PCIE_P1 BY4 / CLKOUT_PCIE_N1 BY3
CLKOUT_PCIE_P0 CN7 / CLKOUT_PCIE_N0 CN8
R1819 60D4R2F-GP — XCLK_BIASREF DJ5

GPP_F19/SRCCLKREQ6# — DU14
GPP_H1/SRCCLKREQ5# — DF23 — SSD_CLKREQ_CPU_N
GPP_H10/SRCCLKREQ4# — DT24 — LAN_CLKREQ_CPU_N
GPP_D8/SRCCLKREQ3# — DT30
GPP_D7/SRCCLKREQ2# — DV30 — WLAN_CLKREQ_CPU_N
GPP_D6/SRCCLKREQ1# — DW30 — GFX_CLKREQ_CPU_N
GPP_D5/SRCCLKREQ0#

XTAL_OUT — DM1 — XTL_38D4M_X2_CPU
XTAL_IN — DL1 — XTL_38D4M_X1_CPU
GPD8/SUSCLK — DW41 — SUS_CLK_CPU
RTCX2 — DT47 — XTL_32K_X2_CPU
RTCX1 — DR47 — XTL_32K_X1_CPU
RTCRST# — DN37 — RTC_RST_N
SRTCRST# — DK37 — SRTC_RST_N

TGL-U-GP-U1
(071.TIGER.0C0U)

LAN_CLKREQ_CPU_N8
SSD_CLKREQ_CPU_N7
GFX_CLKREQ_CPU_N6
WLAN_CLKREQ_CPU_N5
RN1805 — SRN10K-6-GP

3D3V_S0
3D3V_RTC_AUX
RN1802 SRN20KJ-1-GP
SRTC_RST_N
RTC_RST_N
C1803 SCD1U10V2KX-1GP
C1804 SCD1U10V2KX-1GP

XTL_32K_X2_CPU
XTL_32K_X1_CPU
R1811 10MR2J-L-GP
X1801 XTAL-32D768KHZ-88-GP
082.30003.0191
C1802 SC12P50V2JN-2GP
(78.15034.1FL) C1801 SC12P50V2JN-3GP

2020/04/23 SB
C1801 change to 15p

XTL_38D4M_X1_CPU
XTL_38D4M_X2_CPU
R1820 200KR2F-L-GP
X1802 XTAL-38D4MHZ-38-GP
082.30040.0241
C1806 SC12P50V2JN-3GP
C1805 SC12P50V2JN-3GP

2020/02/26 SA
X1802 change from 082.30040.0101 to 082.30040.0241 COMMON PART

EC CMOS CLR
Unmount; only on SA status

RTCRST_ON
Q1802 2N7002K-2-GP
RTC_S
RTC_RST_N
C1807 SCD1U16V2KX-3GP
R1834 100KR2J-1-GP
R1835 2K2R2J-2-GP

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Title: CPU (SPI/LPC/SMBS/XTAL/CLK)
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Audio

27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC
27 HDA_SDIN0_CPU
27 HDA_RST_N_CODEC

Strap
15 HDA_SDOUT_CPU

DMIC

30 DMIC_PCH_CLK
30 DMIC_PCH_DATA

BT

61 NGFF_BT_DISABLE

CNVI

61 PMC_IN
61 PMC_CLK
61 BT_PCMOUT_CLKREQ0
61 BT_PCMFRM_RSTN

Other

20 ME_FWP_SW
24 ME_FWP_ECIO
37 TS_DET_R

24 DGPU_PWROK

7 OF 21

CPU1G

HDA_BITCLK_CODEC — R1904 33R2J-2-GP — HDA_BITCLK_CPU (DR38)
HDA_SYNC_CODEC — R1901 33R2J-2-GP — HDA_SYNC_CPU (DU37)
HDA_SDOUT_CODEC — R1905 33R2J-2-GP — HDA_SDOUT_CPU (DT37)
HDA_SDIN0_CPU (DV37)

GPP_R0/HDA_BCLK/I2S0_SCLK
GPP_R1/HDA_SYNC/I2S0_SFRM
GPP_R2/HDA_SDO/I2S0_TXD
GPP_R3/HDA_SDI0/I2S0_RXD

HDA_RST_N_CODEC — R1928 33R2J-2-GP — HDA_RST_N_CPU (DV41)
PMC_CLK — R1916 33R2F-3-GP — PMC_CLK_CPU (DL53)
BT_PCMFRM_RSTN — R1930 33R2F-3-GP — CNV_RF_RESET_N (DG51)
PMC_IN — R1902 33R2F-3-GP — PMC_IN_CPU (DG50)

GPP_R4/HDA_RST#
GPP_A7/I2S2_SCLK/DMIC_CLK_A0
GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0
GPP_A10/I2S2_RXD/DMIC_DATA1

BT_PCMOUT_CLKREQ0 — R1929 33R2F-3-GP — CLKREQ_CNV (DL49)
DGPU_PWR_EN_CPU (DL52)

GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1
GPP_A11/PMC_I2C_SDA/I2S3_SCLK

TPAD28-2-GP TP1901
NGFF_BT_DISABLE (DH49)

GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0

R1903 200R2F-L-GP — SNDW_RCOMP (DF33)

SNDW_RCOMP

GPP_F8/I2S_MCLK2_INOUT (DW15)
GPP_D19/I2S_MCLK1 (DW23)
TP1902 TPAD28-2-GP

GPP_A23/I2S1_SCLK (DG41) — DGPU_PWROK_PCH — R1938 (G_) 0R2J-2-GP — DGPU_PWROK
GPP_R7/I2S1_SFRM (DT38) — BOARD_ID2
GPP_R6/I2S1_TXD (DW38) — TBT_DET
GPP_R5/HDA_SDI1/I2S1_RXD

GPP_S6/SNDW3_CLK/DMIC_CLK_A0 (DN31) — DMIC_PCH_CLK
GPP_S7/SNDW3_DATA/DMIC_DATA0 (DM31) — DMIC_PCH_DATA

GPP_S 1D8V only
GPP_S4/SNDW2_CLK/DMIC_CLK_A1 (DK33) — SKU_ID
GPP_S5/SNDW2_DATA/DMIC_DATA1 (DK31) — TS_DET_R

GPP_S2/SNDW1_CLK/DMIC_CLK_B0 (DW35) — GPP_S2 — R1939 (G_63.10334.1DL) 0R2J-2-GP
GPP_S3/SNDW1_DATA/DMIC_CLK_B1 (DW35)

GPP_S0/SNDW0_CLK (DT32)
GPP_S1/SNDW0_DATA (DR35)

TGL-U-GP-U1
(071.TIGER.0C0U)

BT_PCMFRM_RSTN — R1931 75KR2J-GP

ID	Description	Setting	Mapping
SKU_ID	GPU function	1	GPU
		0	UMA

1D8V_S5_VCCPRIM
R1906 (G_) 10KR2J-3-GP
SKU_ID
R1907 (U_) 10KR2J-3-GP

ID	Description	Setting	Mapping
TBT_ID	TBT function	1	TBT
		0	NON-TBT
TOUCH_ID	TOUCH	1	no-Touch
		0	Touch

1D8V_S5_VCCPRIM
R1934 10KR2J-3-GP — TS_DET_R
R1937 (R_) 10KR2J-3-GP
1D8V_S5_VCCPRIM
R1935 (TBT_) 10KR2J-3-GP — TBT_DET
R1936 (NONTBT_) 10KR2J-3-GP

Flash Descriptor Security Overide	
MECLR1	Normal = 2-3 pin(default) MEdisable = 1-2 pin

Board ID	Description	Setting	Mapping
ID2	AMP+Scalar	1	W/Scalar
		0	W/Transmitter
ID1	MODE	1	Delphi 238i
		0	Delphi 215i

1D8V_S5_VCCPRIM
R1908 (AMP_) 10KR2J-3-GP — BOARD_ID2
R1911 (NONAMP_) 10KR2J-3-GP
1D8V_S5_VCCPRIM
R1910 (238i_) 10KR2J-3-GP — BOARD_ID1
R1909 (215i_) 10KR2J-3-GP

2019/12/21
Folllow Eiffel215

3D3V_S5
R1915 1KR2J-1-GP
ME_CNTL21

MECLR1
NP1 62.40071.001 SW-SSSS811101-GP
NP2 (DBG_)

ME SW GPIO
1. Resume GPIO
2. Default High

ME_FWP_SW — R1914 (R_) 1KR2J-1-GP — ME_CNTL1 — Q1901 LMBT3906LT1G-1-GP
ME_FWP_ECIO — R1932 1KR2J-1-GP
HDA_SDOUT_CPU

R1933 2K2R2F-GP (R_)
2020/04/08 SD add? for ME loss issue follow copperbox2

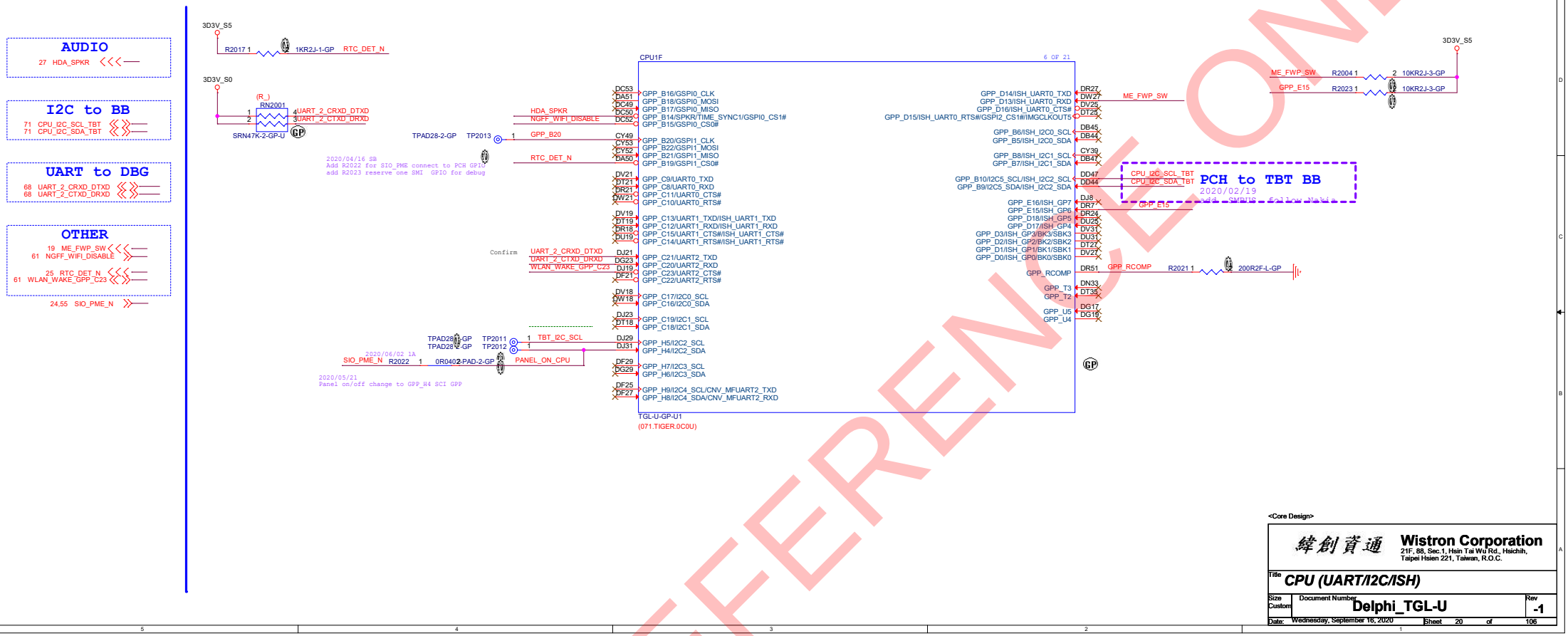
Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Debug mode

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)
Size: Custom | Document Number: Delphi_TGL-U | Rev: -1
Date: Wednesday, September 16, 2020 | Sheet 19 of 106

WISTRON REFERENCE ONLY



WISTRON REFERENCE ONLY

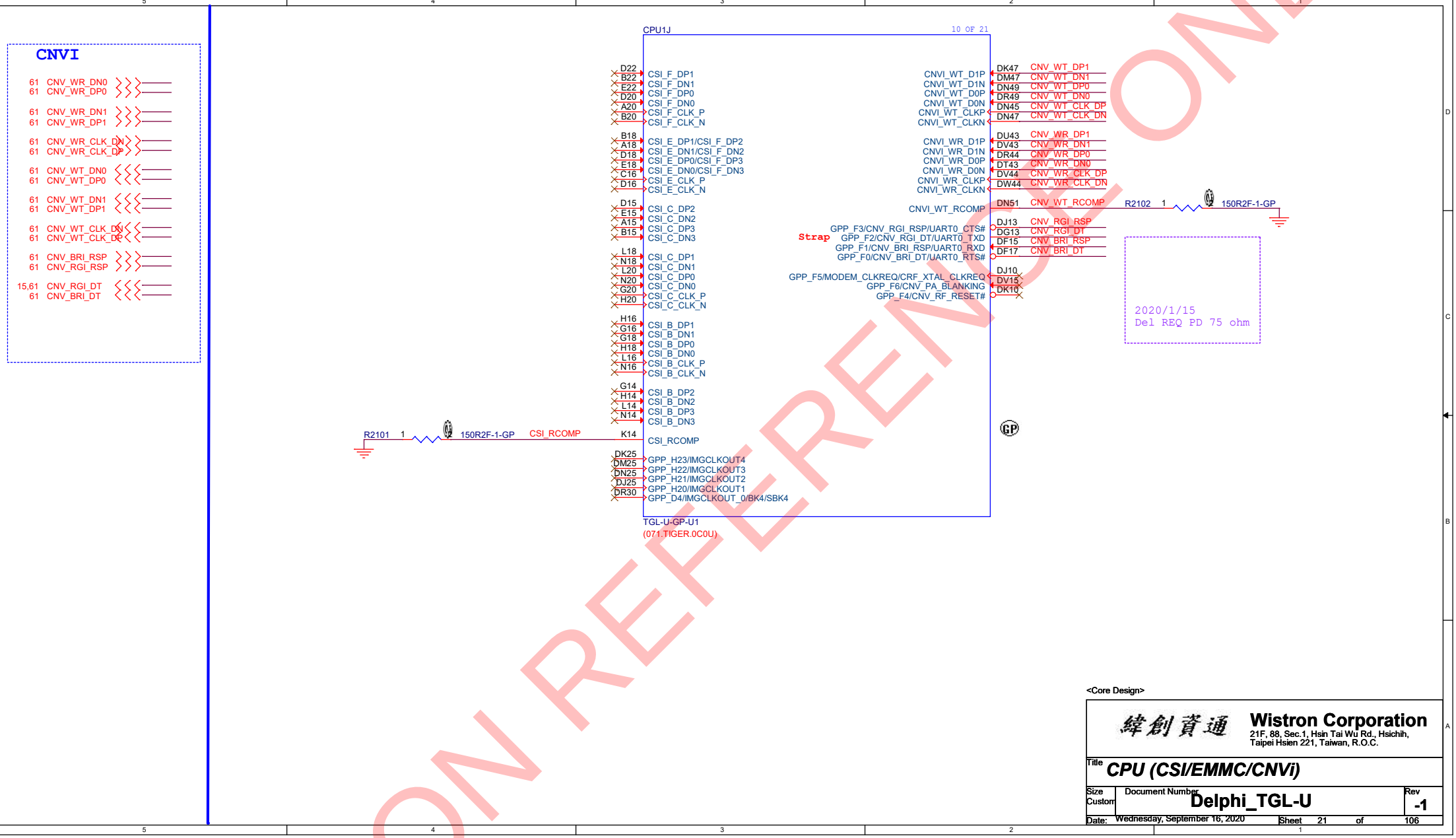
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

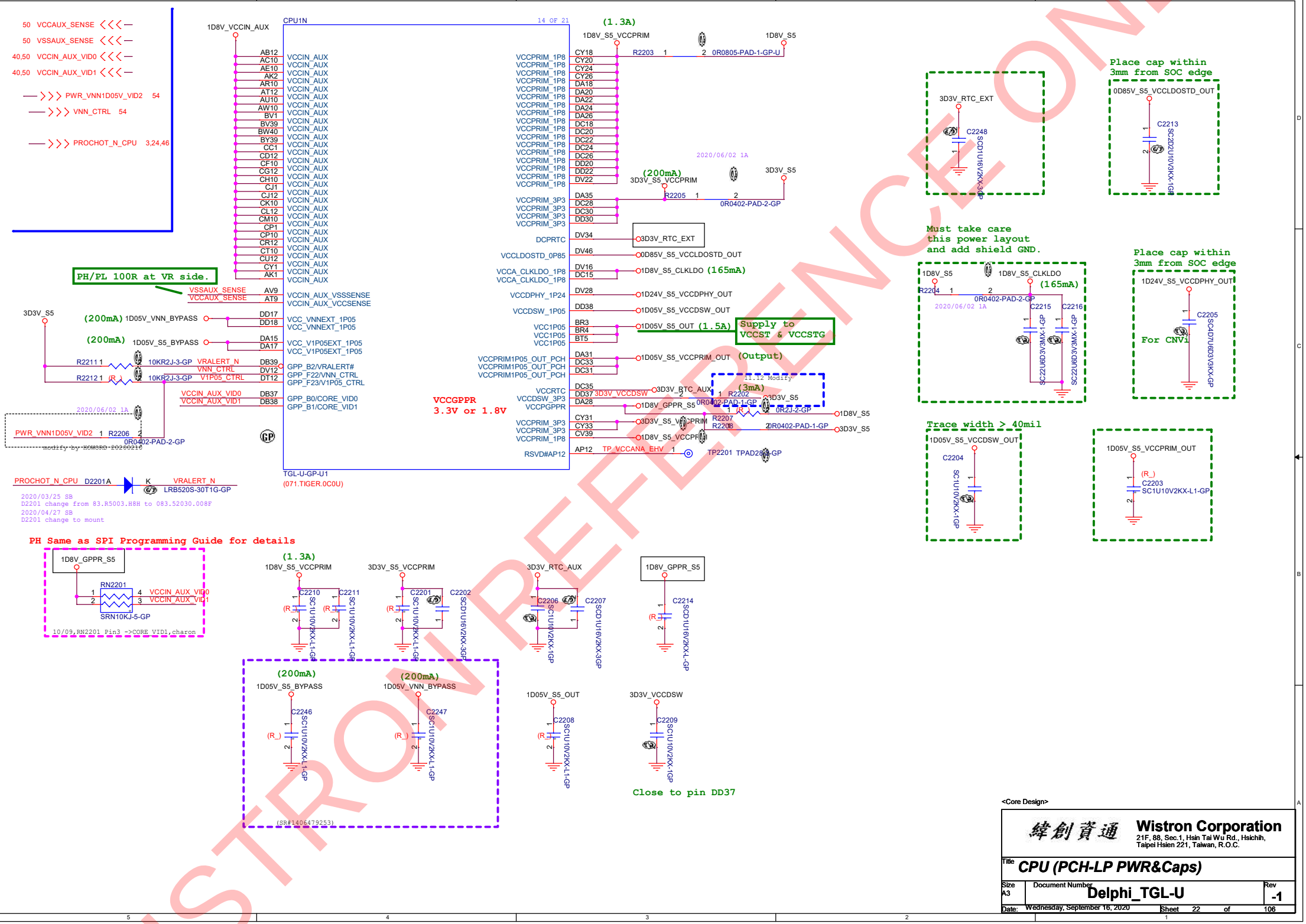
Title: CPU (UART/I2C/ISH)

Size	Document Number	Rev
Custom	Delphi_TGL-U	-1

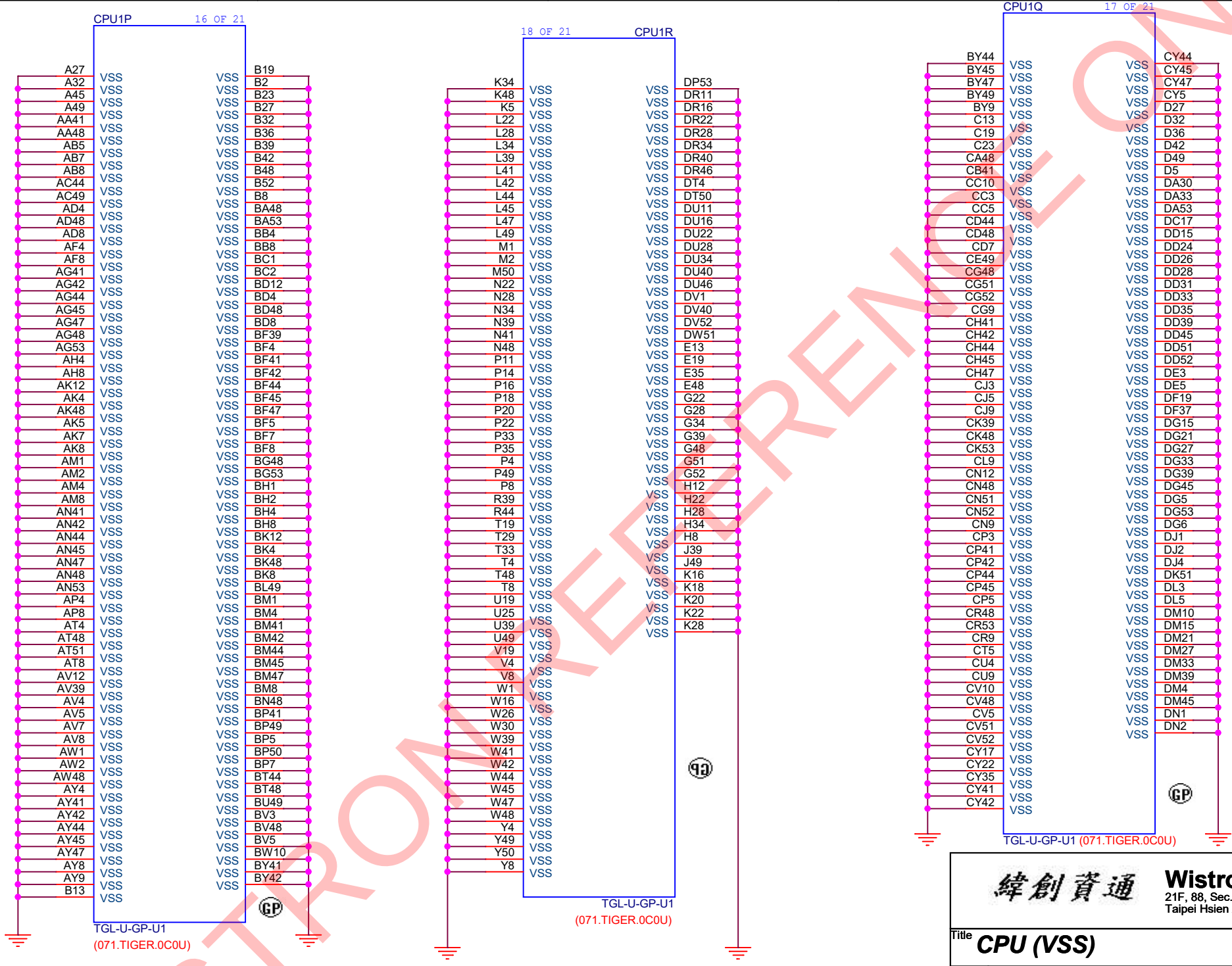
Date: Wednesday, September 16, 2020 Sheet 20 of 106



WISTRON REFERENCE ONLY



WISTRON REFERENCE ONLY



STRONG REFERENCE ONLY

緯創資通

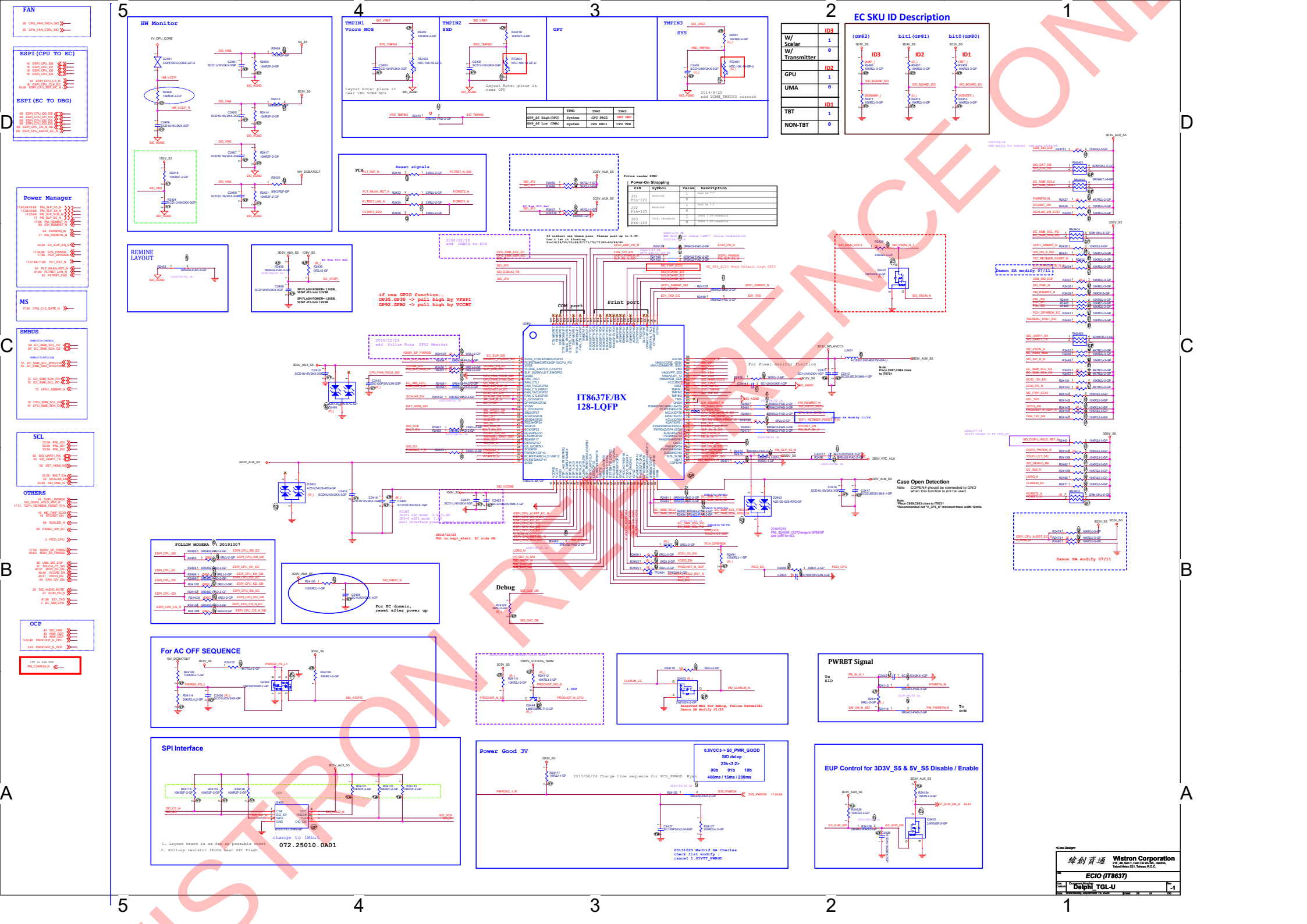
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	**Delphi_TGL-U**	-1

Date: Wednesday, September 16, 2020 Sheet 23 of 106


FAN
ESPI(CPU TO EC)
ESPI(EC TO DBG)
Power Manager
MS
SMBUS
SCL
OTHERS
OCP
HW Monitor
TMPIN1
Vcore MOS
TMPIN2
SSD
GPU
TMPIN3
SYS
EC SKU ID Description
Reset signals
Power-On Strapping
REMINE LAYOUT
if use GPIO function.
GP35_GP30 -> pull high by VFSPI
GP92_GPB2 -> pull high by VCCBT
COM port
Print port
IT8637E/BX
128-LQFP
Debug
Case Open Detection
FOLLOW MOCHERA 20191007
For AC OFF SEQUENCE
SPI Interface
PWRBT Signal
EUP Control for 3D3V_S5 & 5V_S5 Disable / Enable
Power Good 3V
0.8VCC3-> S0_PWR_GOOD
SIO delay:
23h<3:2>
00b 01b 10b
400ms / 15ms / 200ms
For EC domain, reset after power up
change to 1Mbit
072.25010.0A01
Wistron Corporation
ECIO (IT8637)
Delphi_TGL-U
Rev: _1

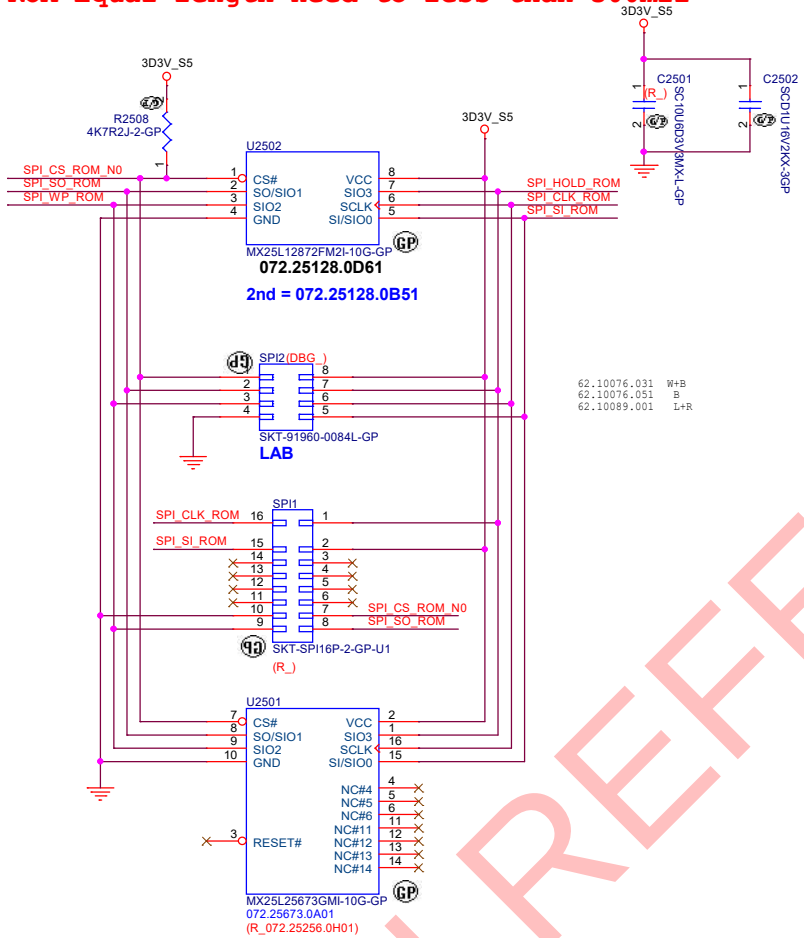
18 SPI_CS_ROM_N0
18 SPI_SO_ROM
15,18 SPI_WP_ROM
15,18 SPI_HOLD_ROM
18 SPI_CLK_ROM
15,18 SPI_SI_ROM

20 RTC_DET_N
18,68 RTC_RST_N

Main Func = SPI Flash

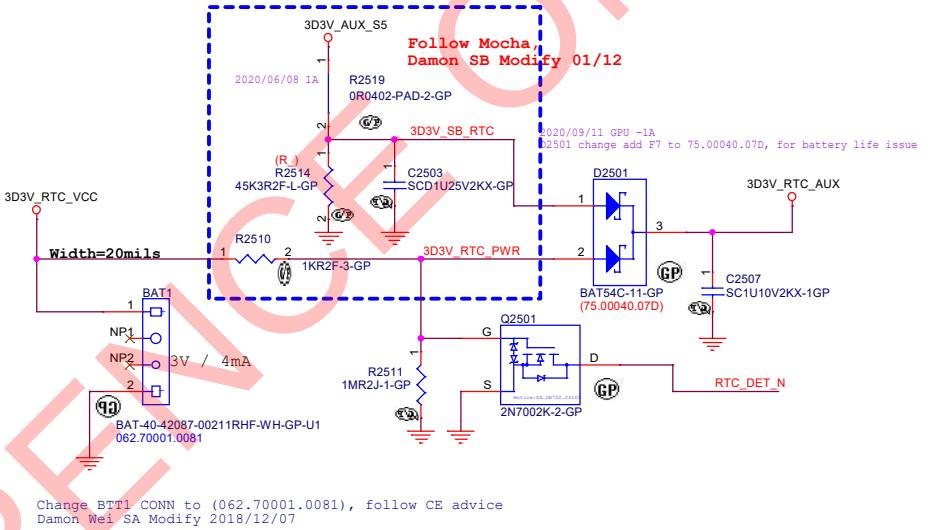
SPI FLASH ROM (16M byte) for PCH

SPI ROM Equal length need to less than 500mil



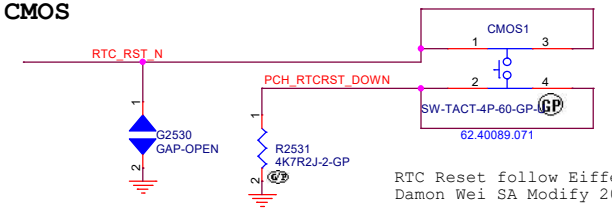
Main Func = RTC

RTC BATTERY



Change BTT1 CONN to (062.70001.0081), follow CE advice
Damon Wei SA Modify 2018/12/07

Clear CMOS



RTC Reset follow Eiffel215i_Kblu
Damon Wei SA Modify 2018/10/18

1-2 short :Clear CMOS
1-2 open : Normal (Default)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

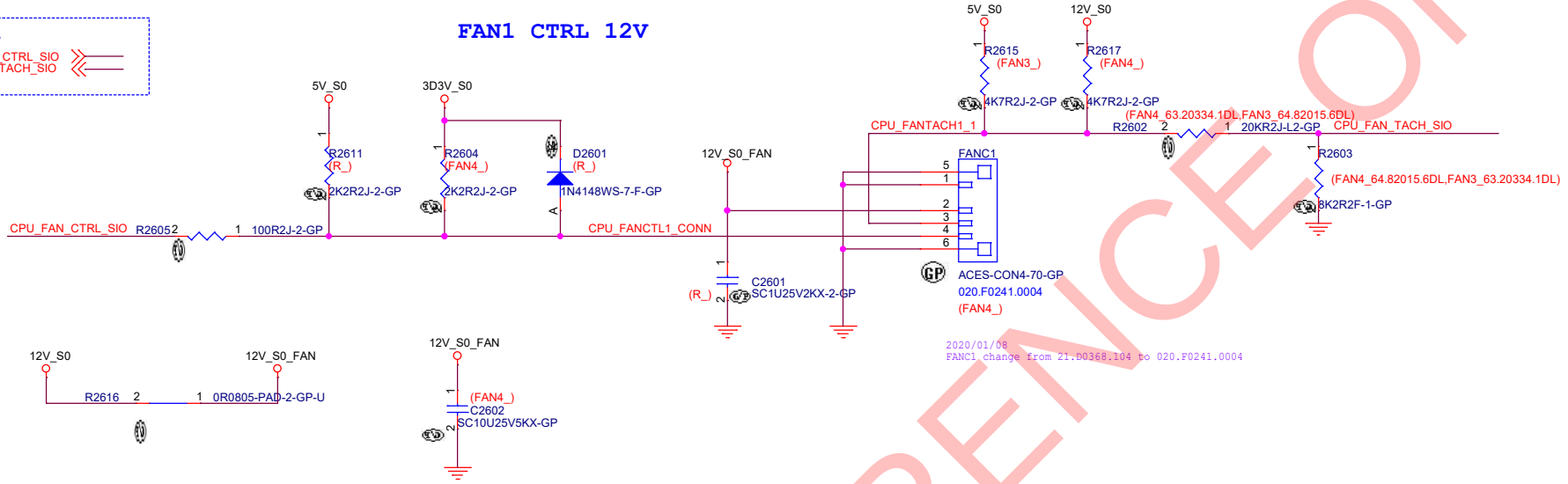
Date: Wednesday, September 16, 2020 | Sheet 25 of 106

WISTRON REFERENCE ONLY

SSID = Thermal

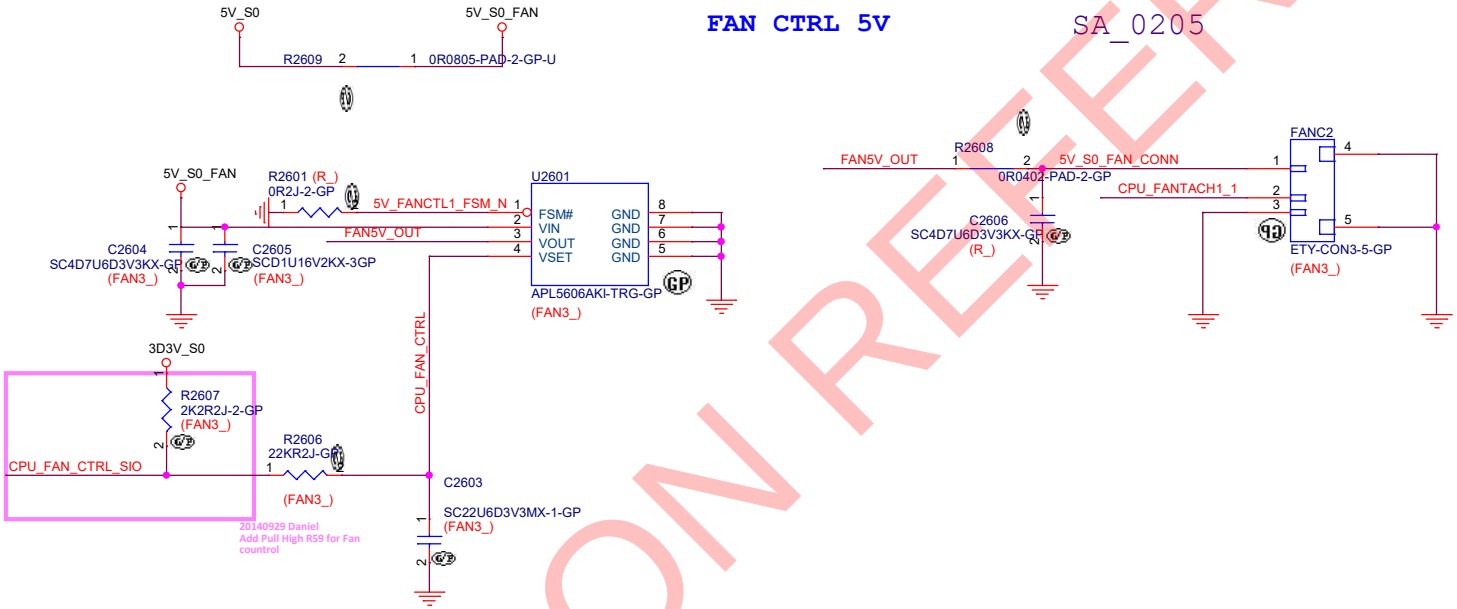
Fan Controller
24 CPU_FAN_CTRL_SIO
24 CPU_FAN_TACH_SIO

FAN1 CTRL 12V



FAN CTRL 5V

SA_0205



<Core Design>

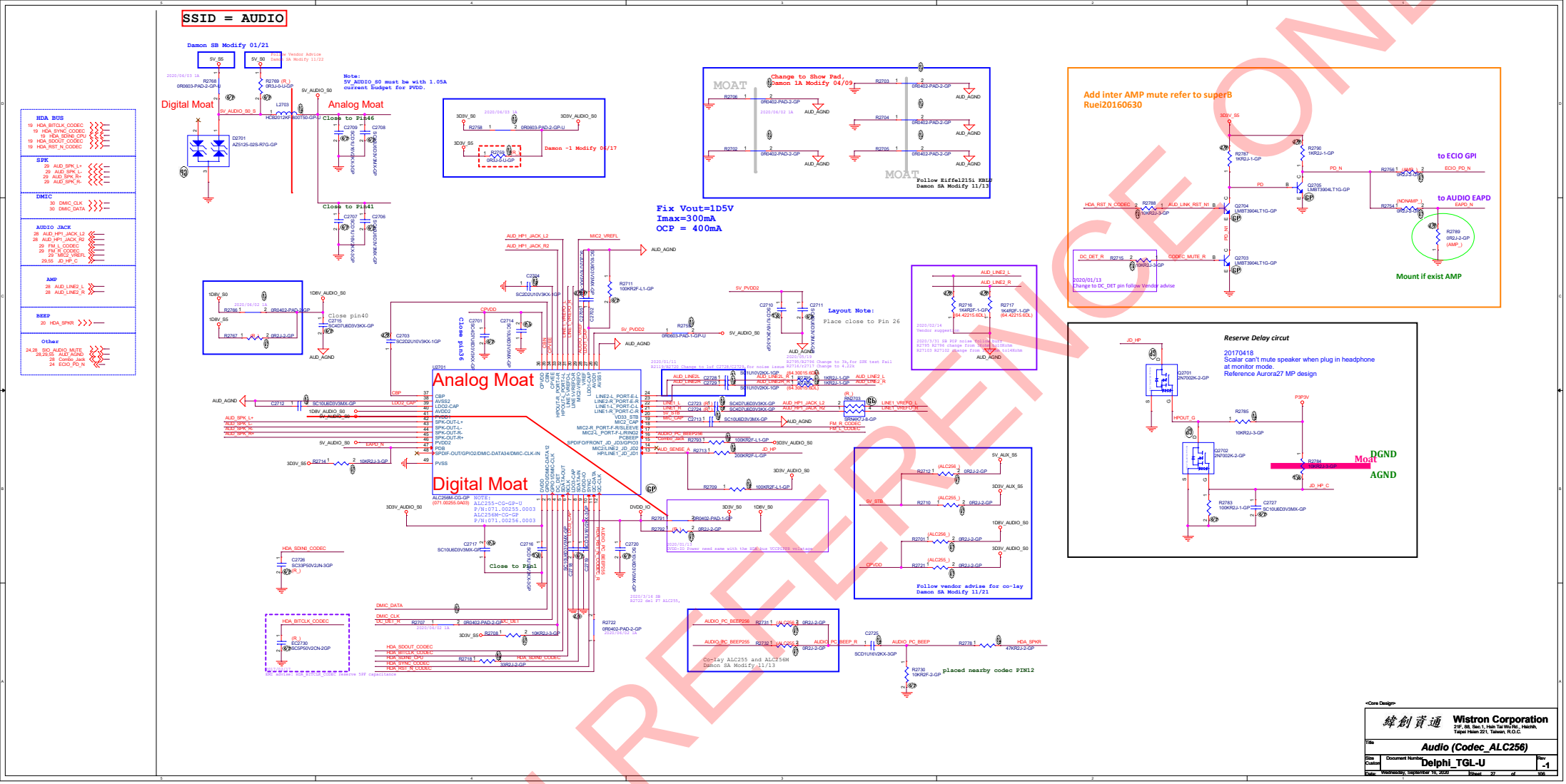
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: B | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 26 of 106

WISTRON REFERENCE ONLY



ONE WISTRON REFERENCE

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

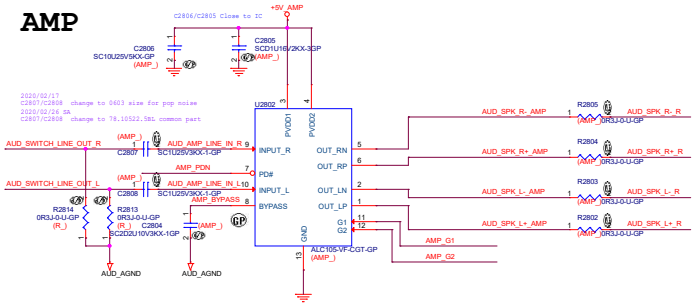
Title: Audio (Codec_ALC256)

Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 27 of 106

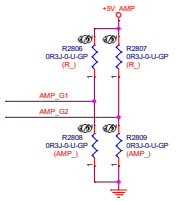
Need check PVDD use 3.3V or 5V

AMP

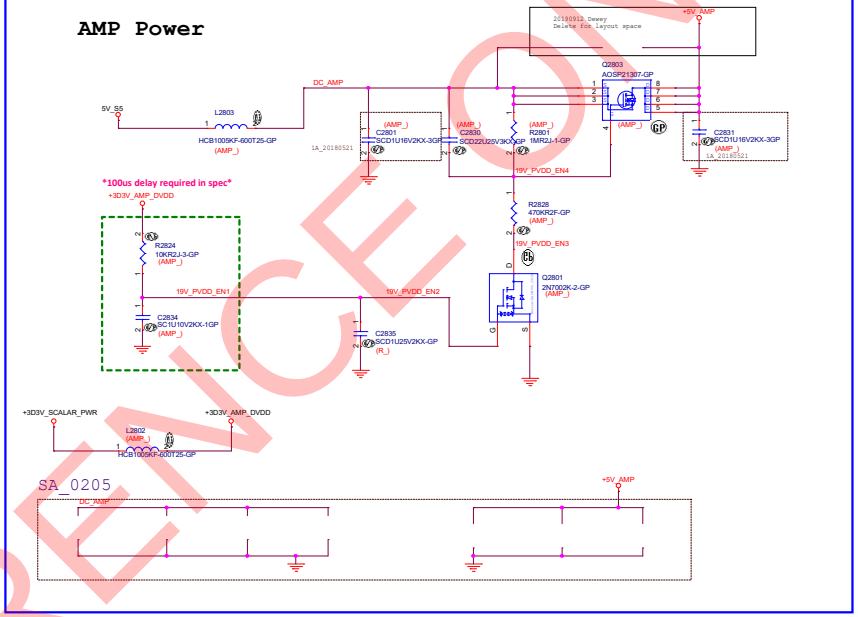


Output Gain Table

G2	G1	Diff-input Mono-output Gain
0	0	11dB Default
0	1	14dB
1	0	19dB
1	1	25dB



AMP Power



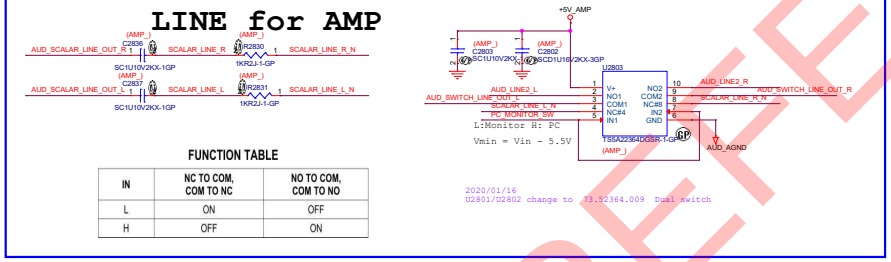
SPK to CONN

29 AUD_SPK_L+_R
29 AUD_SPK_L-_R
29 AUD_SPK_R+_R
29 AUD_SPK_R-_R

AMP Mute

55 SCALAR_AMP_MUTE_N
24 SIO_AUDIO_MUTE
27 Combo_Jack

LINE for AMP



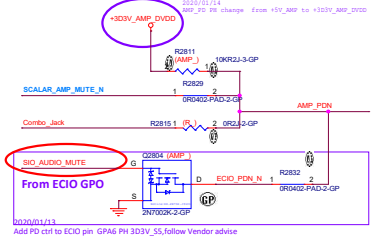
FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

OTHER

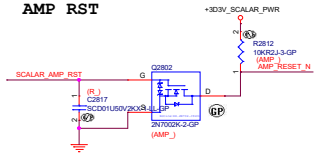
55 PC_MONITOR_SW
55 SCALAR_AMP_RST
27,29,55 AUD_AGND

AMP MUTE



Need to check AMP no rest PIN ?

AMP RST



Audio HP

27 AUD_HP1_JACK_R2
27 AUD_HP1_JACK_L2

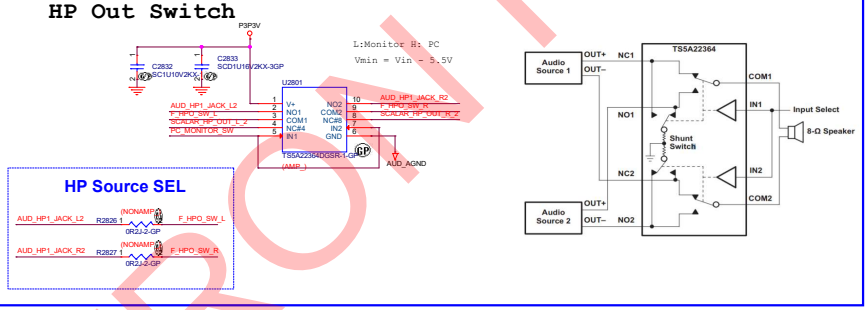
Scalar HP

55 SCALAR_HP_OUT_R_2
55 SCALAR_HP_OUT_L_2

Switch HP

29 F_HPO_SW_L
29 F_HPO_SW_R

HP Out Switch



WISTRON REFERENCE ONLY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (Audio AMP)

Size	Document Number	Rev
Custom	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 28 of 106

SSID = AUDIO Speaker

Need check L and C

SPK Bus

AMP

28 AUD_SPK_L+_R
28 AUD_SPK_L-_R
28 AUD_SPK_R+_R
28 AUD_SPK_R-_R

Audio Code

27 AUD_SPK_L-
27 AUD_SPK_L+
27 AUD_SPK_R-
27 AUD_SPK_R+

AUD_SPK_L+_R — L2904 — MHC1005P121ZBP2A0-GP — AUD_SPK_L+_CON — EC2902 SC1KP50V2KX-1GP

AUD_SPK_L-_R — L2905 — MHC1005P121ZBP2A0-GP — AUD_SPK_L-_CON — EC2903 SC1KP50V2KX-1GP

AUD_SPK_R+_R — L2906 — MHC1005P121ZBP2A0-GP — AUD_SPK_R+_CON — EC2904 SC1KP50V2KX-1GP

AUD_SPK_R-_R — L2907 — MHC1005P121ZBP2A0-GP — AUD_SPK_R-_CON — EC2905 SC1KP50V2KX-1GP

2020/02/26 SA
L2904,L2905,L2906,L2907 change to 068.00049.0041

2020/01/10
SPK1 change from 020.F1076.0004 to 020.F0420.0004

SPK1 — ACES-CON4-85-GP — 020.F0420.0004

AUD_SPK_L+ — R2906 — (NONAME) 0R3J-0-U-GP — AUD_SPK_L+_R
AUD_SPK_L- — R2907 — (NONAME) 0R3J-0-U-GP — AUD_SPK_L-_R
AUD_SPK_R+ — R2908 — (NONAME) 0R3J-0-U-GP — AUD_SPK_R+_R
AUD_SPK_R- — R2909 — (NONAME) 0R3J-0-U-GP — AUD_SPK_R-_R

AUD_SPK_L- / AUD_SPK_L+ — ED2901 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.00353.0A7D
3rd = 075.52215.007D

AUD_SPK_R- / AUD_SPK_R+ — ED2902 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.00353.0A7D
3rd = 075.52215.007D

Audio Jack Bus

27 FM_L_CODEC
27 FM_R_CODEC
27 MIC2_VREFL

28 F_HPO_SW_L
28 F_HPO_SW_R

27,55 JD_HP_C

27,28,55 AUD_AGND

MIC2_VREFL — R2901 2K2R2J-2-GP — R2903 2K2R2J-2-GP

PCB trace width of RING2 & SLEEVE at least 40 mil

FM_L_CODEC — L2911 — MHC1005P121ZBP2A0-GP — RING2
FM_R_CODEC — L2910 — MHC1005P121ZBP2A0-GP — SLEEVE

2020/02/26 SA
C2903/C2927 change to 78.10224.2FL common part

C2903 SC680P50V2KX-2GP — C2927 SC680P50V2KX-2GP — AUD_AGND

F_HPO_SW_L — R2904 75R2J-1-GP — AUD_HP1_JACK_L2_R — L2903 — MHC1005P121ZBP2A0-GP — AUD_HP1_JACK_L1
F_HPO_SW_R — R2905 75R2J-1-GP — AUD_HP1_JACK_R2_R — L2902 — MHC1005P121ZBP2A0-GP — AUD_HP1_JACK_R1

AUD_HP1_JD_TYPE
JD_HP_C

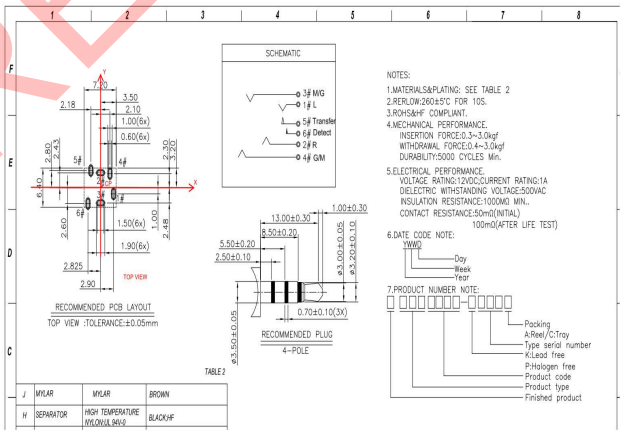
AUDS1 — AUDIO-JK600-GP — 022.10002.0K41 (022.10002.0C41)

2020/02/26 SA
L2902,L2903 change to 068.00049.0041

EC2912 SC1KP50V2KX-1GP — EC2911 SC1KP50V2KX-1GP — EC2910 SC1KP50V2KX-1GP — AUD_AGND

2020/01/16
AUDS1 change 022.10002.0C41 from to 022.10002.0K41
add F7 to 022.10002.0C41, ME symbol OBS

HP-Out-Right
HP-Out-Left
Ring2
Sleeve



AUD_HP1_JACK_R1 / AUD_HP1_JACK_L1 — ED2903 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.00353.0A7D
3rd = 075.52215.007D

AUD_HP1_JD_TYPE / JD_HP_C — ED2904 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.00353.0A7D
3rd = 075.52215.007D

RING2 / SLEEVE — ED2905 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.00353.0A7D
3rd = 075.52215.007D

AUD_HP1_JD_TYPE — 2020/06/02 1A — R2902 0R0402-PAD-2-GP — AUD_AGND

Follow Eiffel215 KBLU
Damon SA Modify 11/15

AUDIO MUTE

2020/01/14
Del Mute circuit, Layout placement not enough

WISTRON REFERENCE ONLY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

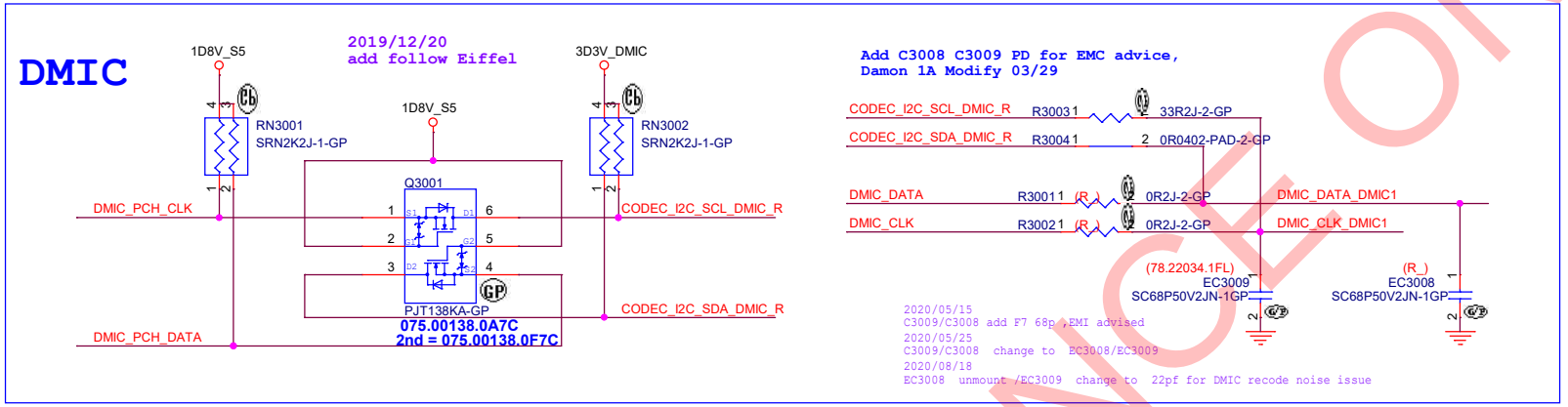
Title: Audio (Speaker/HPMIC)

Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 29 of 106

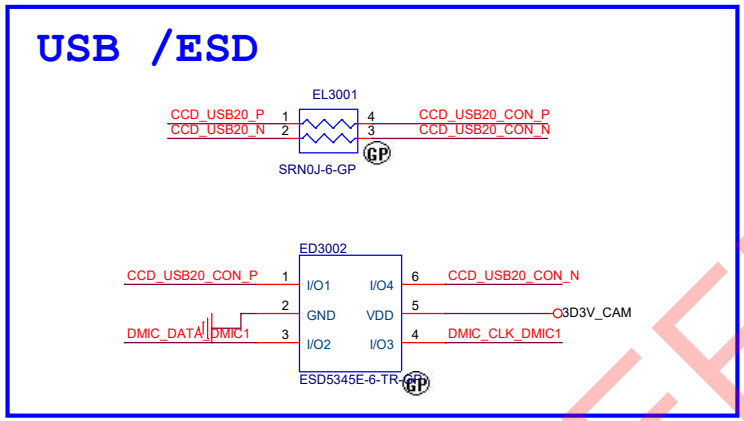
DMIC

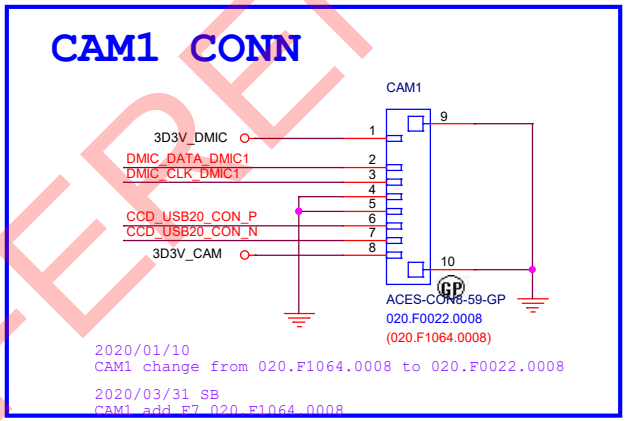
27 DMIC_DATA
27 DMIC_CLK
19 DMIC_PCH_CLK
19 DMIC_PCH_DATA

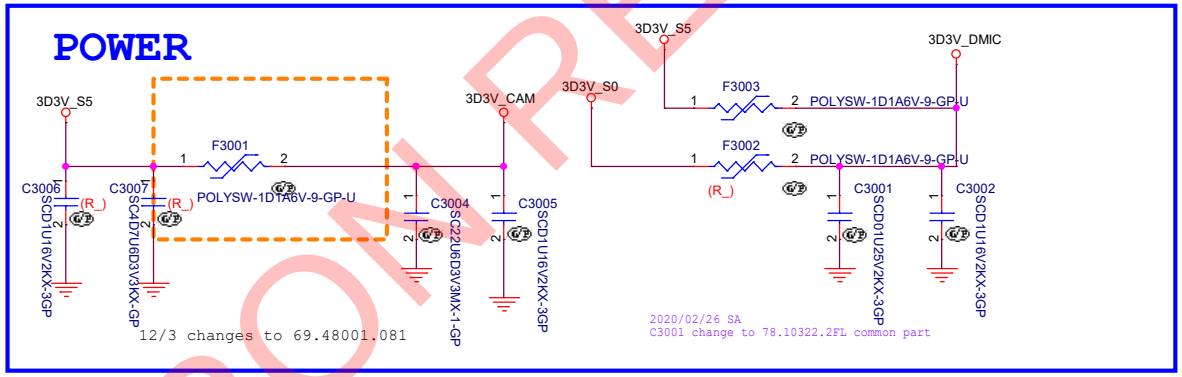


USB

16 CCD_USB20_N
16 CCD_USB20_P







WISTRON REFERENCE ONLY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (Webcam/DMIC)

Size: B | Document Number: Delphi_TGL-U | Rev: -1

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Giga LAN

PCIE

16 LAN_PCIE_TX_N
16 LAN_PCIE_TX_P
16 LAN_PCIE_RX_N
16 LAN_PCIE_RX_P
16 LAN_CLK_CPU_N
16 LAN_CLK_CPU_P
18 LAN_CLKREQ_CPU_N
17 LAN_WAKE_N
24,89 PLTRST_LAN_N
17,24,68,71,89 PLT_RST_N

Bogis 20121222
Change solution to
RTL8111GA

Colse to the AVDD33 pin location

C302 close to Pin11 (AVDD33)

Colse to the AVDD10 pin location

Colse to the pin22

Reserve for RTL8111G/GS/GA

Reserve for RTL8111GA

Mount for RTL8111G /RTL8111H

Mount for RTL8111GS/RTL8111GA ONLY

2018/01/03 Damon 1A Modify

Close to LAN chipset

M:Mount	R:Reserved			
IC	P/N	L3101	R3103	C3147
RTL8111GA	71.08111.Y03	M	R	M
RTL8111GS	71.08111.T03	M	R	M
RTL8111G	71.08111.U03	R	M	R
RTL8111H	071.8111H.0003	R	M	R

Change to 68.IH601.301 Vendor advice
Damon Wei SA Modify 20190114

2014/09/01 Daniel
Follow Lijiang LAN Surge Solution Cost Down

Unmount EC3101 ~ EC3108, follow Vendor Request.
Damon Wei SA Modify 2017/11/10

XTAL

X3101
082.30005.0A81 HARMONY
082.30005.0911 MURATA
082.30005.0931 TXC

12/4 Derek remove R273 short pad

2017/09/15 Only Mount C3118,C3119
Damon Wei SA Modify

Connect to SIO GPIO
S3/S4/S5 = Low
Others = High
To meet Tpvpgrl spec > 100ms
(Power Stable to PERST Inactive

Check with Kelia the LAN reset issue

EMI

ESD

75.01215.07C

2017/04/29
ED3203/ED3204/ED3205/ change to (75.00099.07G),F7 for common part

WAKE

Davy 0712
Leakage from LAN_WAKE# to 3D3V_LAN
1K 0.4V --> 10K 0.054V

Layout close to
CPU/FCH/PCH

Lan WAKE follow Steffi
2017/10/12 Damon SA Modify

LED

2011/06/26

Lan Surge

2014/09/01 Daniel
Follow Lijiang LAN Surge Solution Cost Down

PCB

Act Link

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

LAN Power

Modify LAN PWR delay circuit,for Rising time >1ms
Damon Wei 1A 19/04/08

+3VM_LAN rise time:
0.5mS ~ 100mS.

S0:3D3V_S5
S3:3D3V_S5
S4:3D3V_S5
S5:3D3V_S5
EUP:0

RJ1 CON

2016/12/27
RJ1 symbol change to 062.10005.0371

<Variant Name>

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Title: LAN (RSVD)
Size: Custom
Document Number: Delphi_TGL-U
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Date: Wednesday, September 16, 2020
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LAN (RSVD) (RJ45+Trans)

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USB Port7 -> Card Reader

USB 2.0

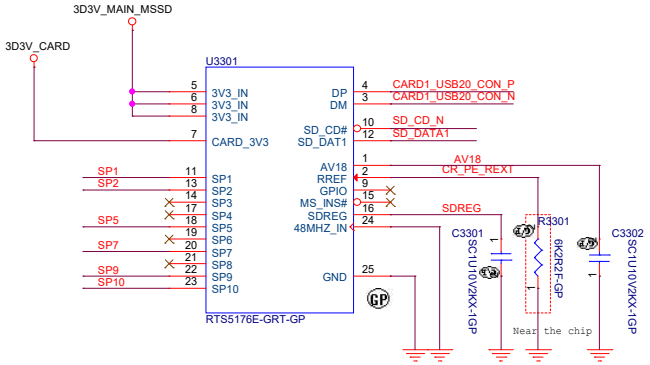
16 CARD1_USB20_P
16 CARD1_USB20_N

2IN1 (SD/MMC) Combo Net

SP1	SD_WP
SP2	SD_DATA0
SP5	SD_CLK
SP7	SD_CMD
SP9	SD_DATA3
SP10	SD_DATA2

SA 0205

SD_WP
SD_DATA0_1
SD_DATA1_1
SD_DATA2
SD_DATA3
SD_CLK_1
SD_CMD
SD_CD_N



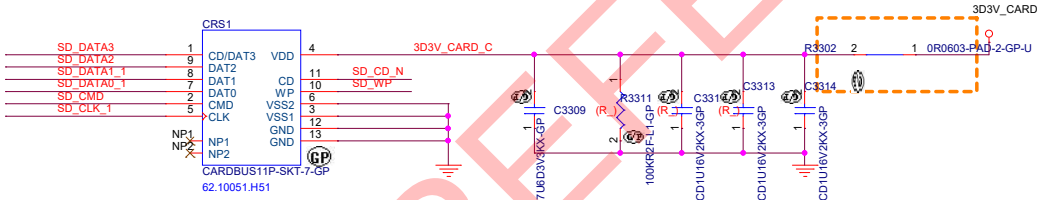
EMI/ESD near Chip

EMI reserve

2020/06/03 1A

SD_DATA0	R3303 1	2 0R0402-PAD-2-GP	SD_DATA0_1
SD_DATA1	R3304 1	2 0R0402-PAD-2-GP	SD_DATA1_1
SD_CLK	R3305 1	2 0R0402-PAD-2-GP	SD_CLK_1

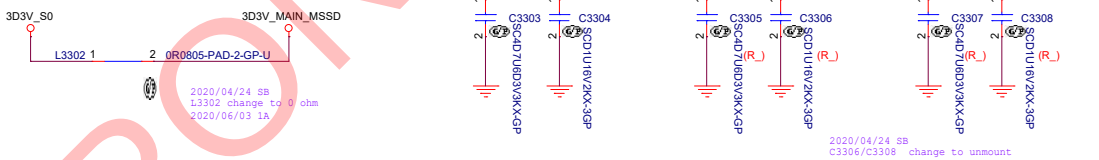
2IN1 CONN (SD/MMC)



2019/12/24
CRS1 62.10051.H51 change to 062.10002.0561

2019/12/24
CRS1 change to 62.10051.H51

RTS5176E Power



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Size: Custom | Document Number: Delphi_TGL-U | Rev: -1
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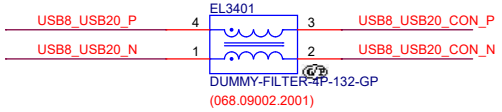
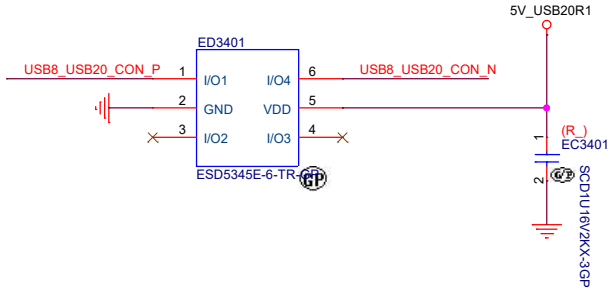
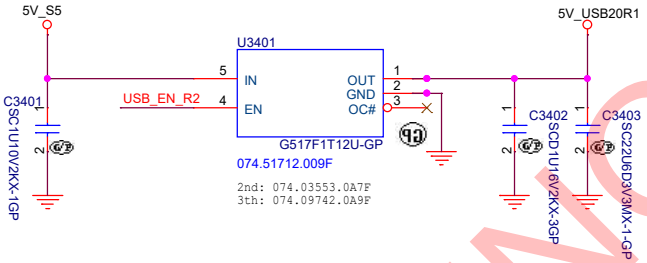
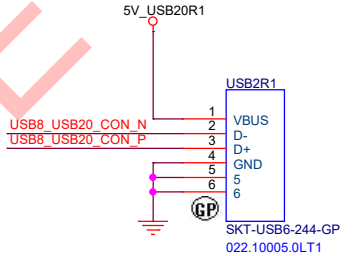
USB Port8 -> USB2.0 CONN

16 USB8_USB20_N
16 USB8_USB20_P
35 USB_EN_R2









2017/02/18
USB2R1 change to 022.10005.0LT1

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Title: USB3.1 GEN2

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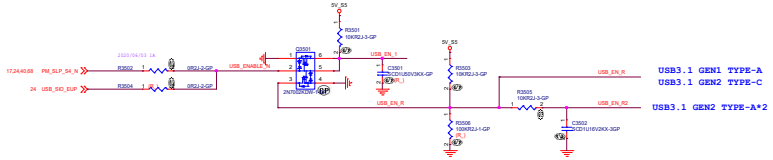
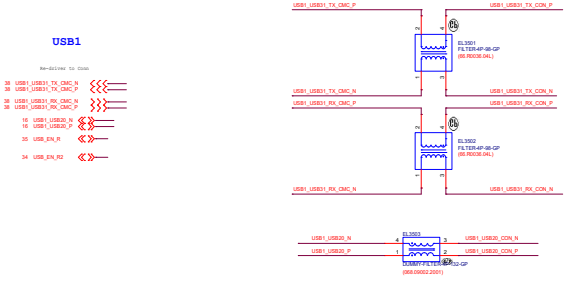
USB Power Enable

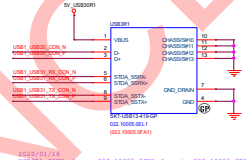
	S5	S4	S3-S0		S5	S4	S3-S0	Status
PM_SLP_S4_N	L	L	H	USB_SIO_EUP	L	L	H	No Support S4/S5 USB wake up
				USB_SIO_EUP	H	H	H	Support S3/S4/S5 USB wake up



USB1 GEN2

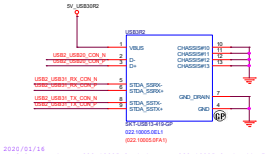


USB3.1 GEN2 TYPE-A

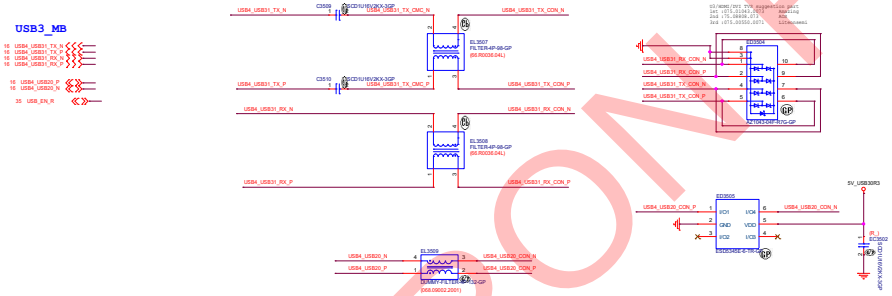


USB2 GEN2

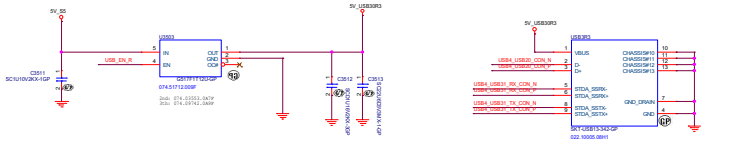
USB3.1 GEN2 TYPE-A



USB3 GEN1



USB3.1 GEN1 TYPE-A



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Title
USB (USB Charger)

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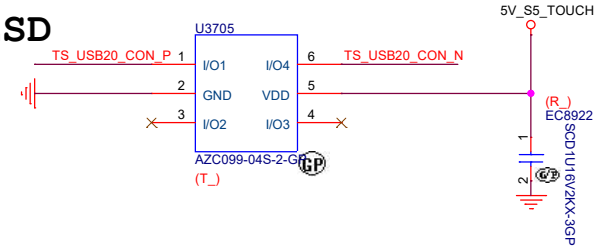
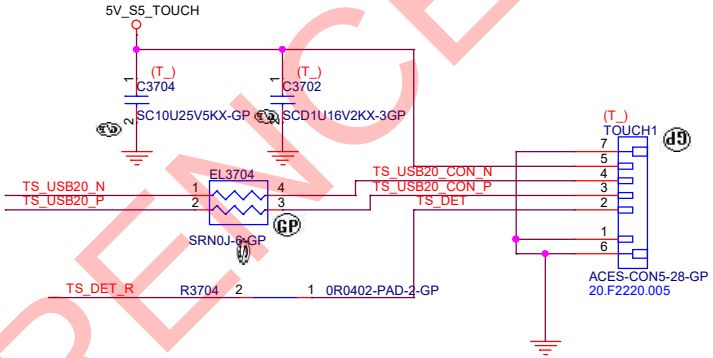
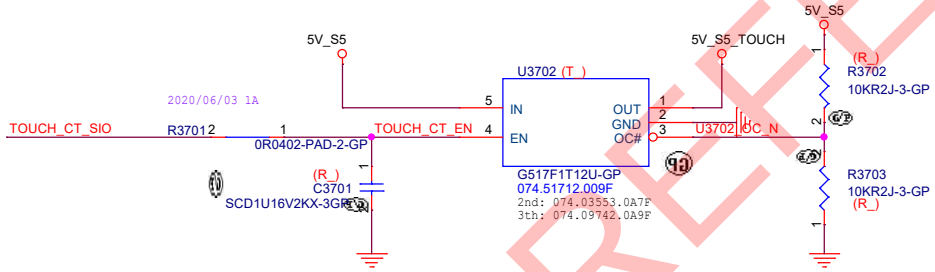
USB Port5 -> Touch

16,37 TS_USB20_N
16,37 TS_USB20_P
24 TOUCH_CT_SIO
19 TS_DET_R

ESD







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Title: ***USB (RSVD)***

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Re-Driver PI3EQX1004

USB1
USB3.2 Type-A Port1

CPU to Re-driver

16 USB1_USB31_TX_P
16 USB1_USB31_TX_N
16 USB1_USB31_RX_P
16 USB1_USB31_RX_N

Re-driver to Conn

35 USB1_USB31_TX_CMC_P
35 USB1_USB31_TX_CMC_N
35 USB1_USB31_RX_CMC_P
35 USB1_USB31_RX_CMC_N

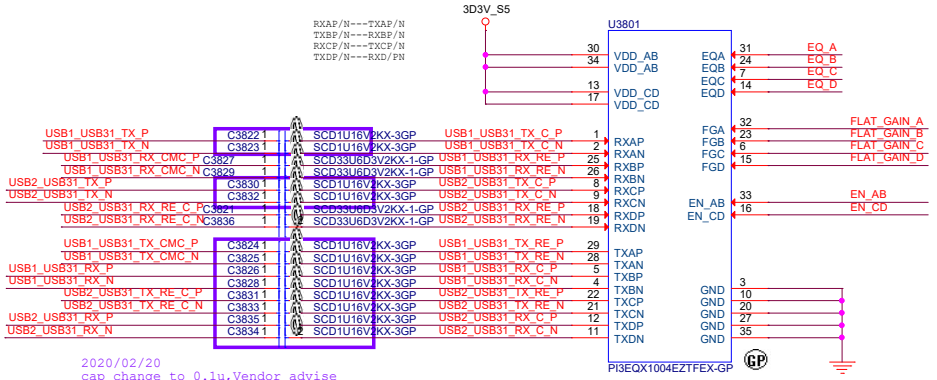
USB2
USB3.2 Type-A Port2

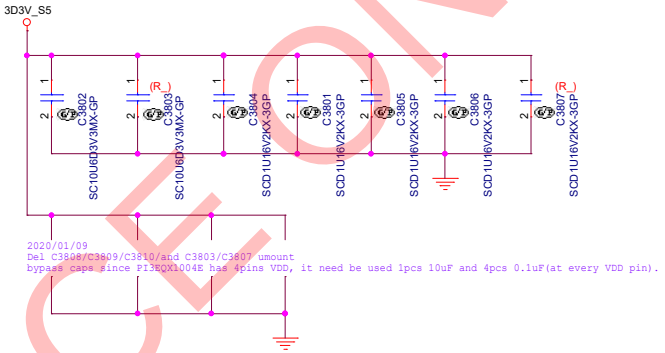
CPU to Re-driver

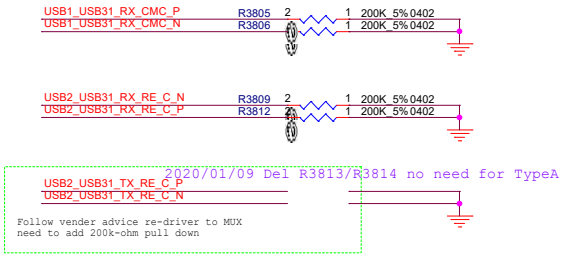
16 USB2_USB31_TX_P
16 USB2_USB31_TX_N
16 USB2_USB31_RX_P
16 USB2_USB31_RX_N

Re-driver to Conn

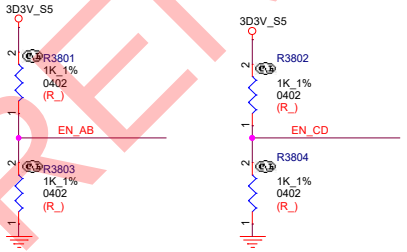
35 USB2_USB31_TX_RE_C_P
35 USB2_USB31_TX_RE_C_N
35 USB2_USB31_RX_RE_C_P
35 USB2_USB31_RX_RE_C_N



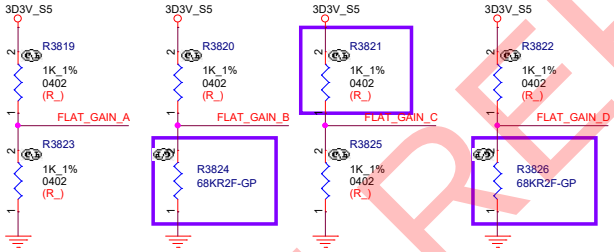




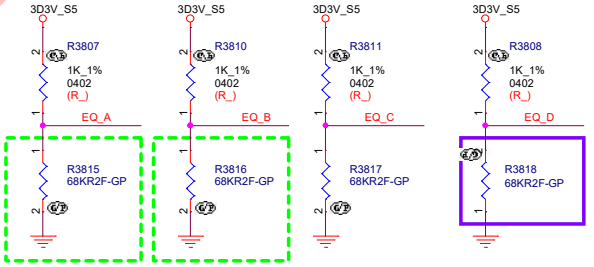
Channel Enable Setting



FLAT_GAIN



EQ GAIN



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Title	USB (RSVD)
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Title: ***Sequence (RSVD)***

Size	Document Number	Rev
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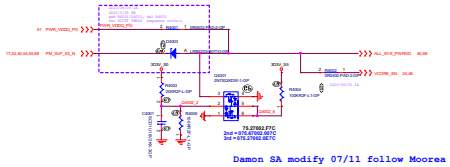
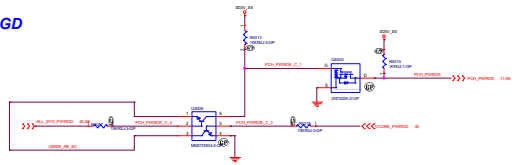
Power Sequence

VCORE_EN

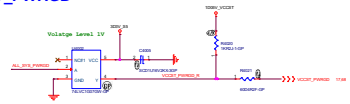


Damon SA modify 07/11 follow Moorea

VCORE_PWRGD

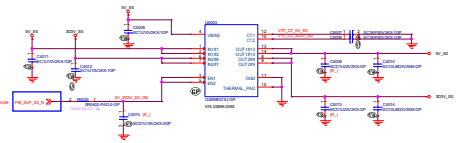


VCCST_PWRGD

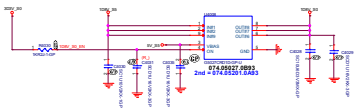


VCCST_PWRGD circuit follow Lenny
Rosa2.0 SA Modify 1004

3D3V_S0 & 5V_S0



1D8V_S0



1D8V_ES1_ONLY

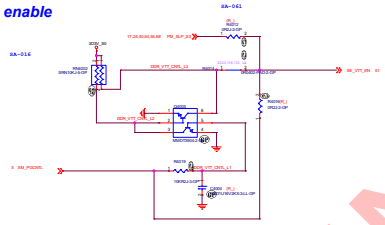
2020/06/02 1A
Del 1D8V_ES1_ONLY circuit

DDR4 Power Sequence

VPP(2.5V) enable

VDDQ(1.2V) enable

VTT(0.6V) enable



1D05V_VCCST_EN

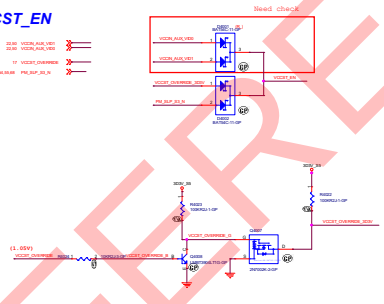
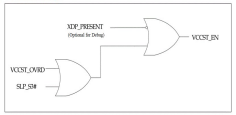


Figure 231. VCCST Enable Logic



1D05V_VCCST/1D05V_VCCSTG

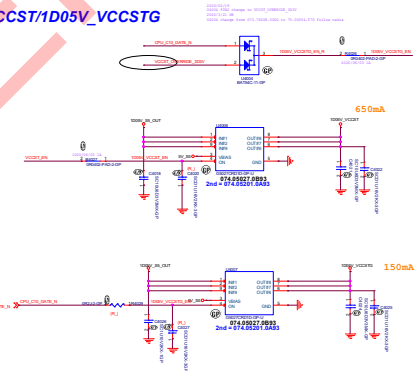
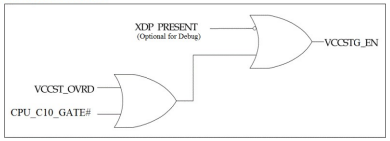


Figure 232. VCCSTG Enable Logic



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Title: ***Sequence (RSVD) (DS3/S0ix)***

Size	Document Number	Rev
A	Delphi_TGL-U	-1

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Title: ***INT IO (RSVD)***

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A	Delphi_TGL-U	-1

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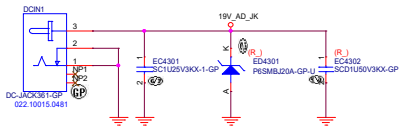
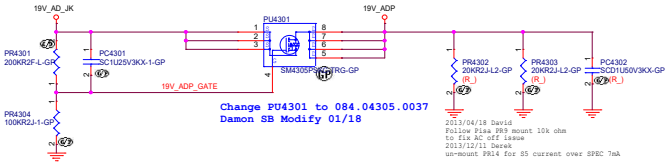
DC Jack



2020/3/31 SB
DC in TVS and cap-- EC4301/ED4301 Add F7 (R_)
2020/5/20
EC4301 change mount 1uf, EMI advised

Soft start

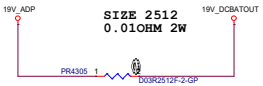


Change PU4301 to 084.04305.0037
Damon SB Modify 01/18

2013/04/18 David
Follow Pisa PR3 mount 10k ohm
to fix AC off issue
2013/12/11 Derek
un-mount PR14 for S5 current over SPEC 7mA

2020/02/26 SA
EC4301,PC4301 change to 78.10522.58L common part

OCP

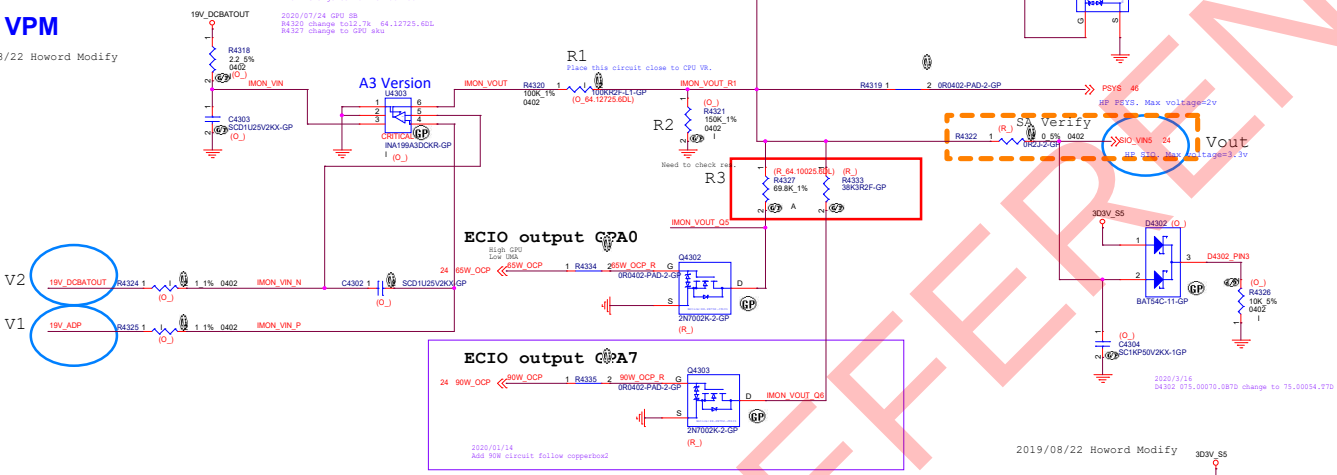


2020/07/10 for UMA ocp setting
PR4305 change to 0.005R
R4320change to 16.5K
R4333 change to unmount
R4319 change to mount
2020/07/24 GPU SB
R4327 change to 10k for 90W OCP

2020/07/24 GPU SB
R4320 change to12.7k 64.12725.6DL
R4327 change to GPU sku

VPM

2019/08/22 Howord Modify



2020/01/14
Add 90W circuit follow copperbox2

2020/3/16
D4302 075.00070.0B7D change to 75.00054.T7D

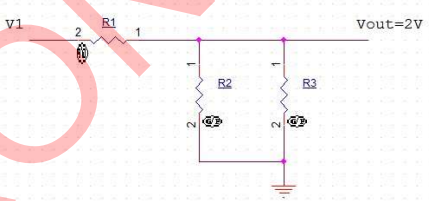
65W ADP
V=I*PR4101*gain
3.08*0.005*200=3.08V

90W ADP
V=I*PR4101*gain
4.26*0.005*200=4.26V

135W ADP
V=I*PR4101*gain
6.39*0.005*200=6.39V

180W ADP
V=I*PR4101*gain
8.53*0.005*200=8.53V

ADP	180	135	90	65
I	9.47	7.11	4.74	3.42
OCP(I)	8.53	6.39	4.26	3.08
Gain	200	200	200	200
R	0.005	0.005	0.005	0.005
V1	8.53	6.39	4.26	3.08
PSYS	2	2	2	2
R1	100	100	100	100
R2	185.37	185.37	185.37	185.37
R3	36.71	60.32	168.89	0
Rth(R2//R3)	30.65	45.51	88.37	185.37



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (DC IN/BAT CON)

Size	Document Number	Rev
Custom	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 43 of 108

WISTRON REFERENCE ONLY

(Reserved)

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<Core Design>

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

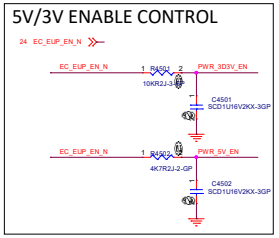
Title: ***BUCKBOOST(ISL9538H)***

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 44 of 106

OFFPAGE-Signal

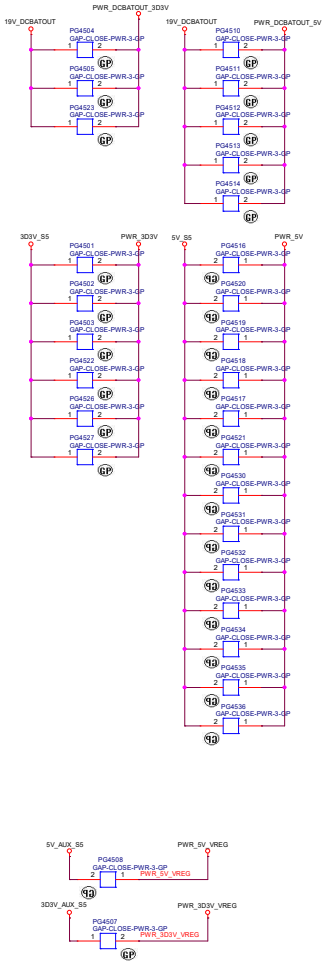
5V/3V ENABLE CONTROL



PH on EE Side

153 PWR_3D3V_5V_PG

OFFPAGE-GAP



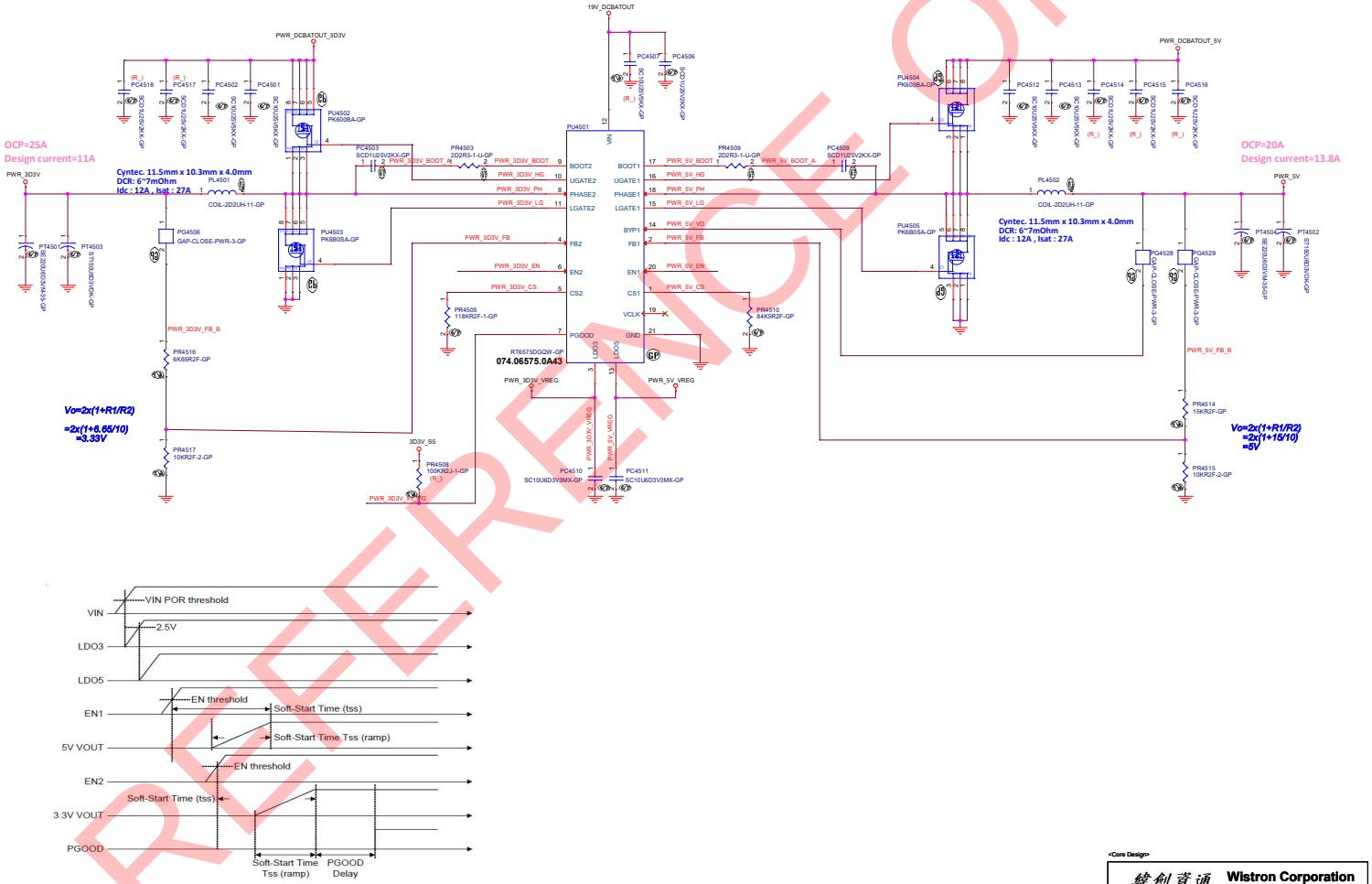


Figure 6. RT6575B Timing

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Title: POWER (RT6575D_5V/3D3V_S5)

Size	Document Number	Rev
Custom	Delphi TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 45 of 106

OFFPAGE
Check PIC-EE

Reserve for Power test

ICL
VBOOT=1.8V
Fsw=568kHz@VIN=7.4V
ICCMAX=72A
Disable QR
Disable DVID LIFT

TGL
VBOOT=0V
Fsw=568kHz@VIN=7.4V
ICCMAX=66A
Disable QR
Disable DVID LIFT

ICL IccMax=69A 500KHz Vboot=0V

	2 Phase	3 Phase
PR4619	71.5K	71.5K
PR4666	2.55K	110K
PR4624	16.5K	16.5K
PR4669	3.32K	0.562K

TGL_28W測試單板 VBOO T = 1.8V
2 Phase
PR4619 = 43.2Kohm
PR4666 = 1.4Kohm
PR4624 = 11.8Kohm
PR4669 = 10ohm

3 Phase
PR4619 = 107Kohm
PR4666 = 1.4Kohm
PR4624 = 10.2Kohm
PR4669 = 10ohm

TGL_15W單板測試VBOOT = 1.8V
PR4619 = 1.4 kohm
PR4666 = 3.92 kohm
PR4624 = 2.87 kohm
PR4669 = 10 ohm

VR_HOT Thermal_Alert#	100C/97C	Lily 120C/100C
PR4627	24.9K	36.5K
PR4622	12.4K	17.8K
PR4701	110K	3.48K

電感3高 0.9mohm	ICL IccMax=72A	TGL IccMax=66A
PR4601	26.7K	30.1K
PR4665	2.87K	2.05K
PR4643	17.8K	18.7K

	電感3高 0.9mohm	電感4高 0.66mohm
PR4628 PR4633	2K	2K
PR4655 PR4646	2K	2K
PR4662 PR4663	2.61K	4.64K

0603 Size

	2 Phase	3 Phase
PR4645	上件	DY
PR4673	上件	DY

電感3高 0.9mohm	ICL IccMax=72A	TGL IccMax=66A
PR4640	31.6K	34K

LL/IMON Compesation
NCP15XH103F03RC
Need confirm with RT If you change Chock
Close to PL4701

<Core Design>

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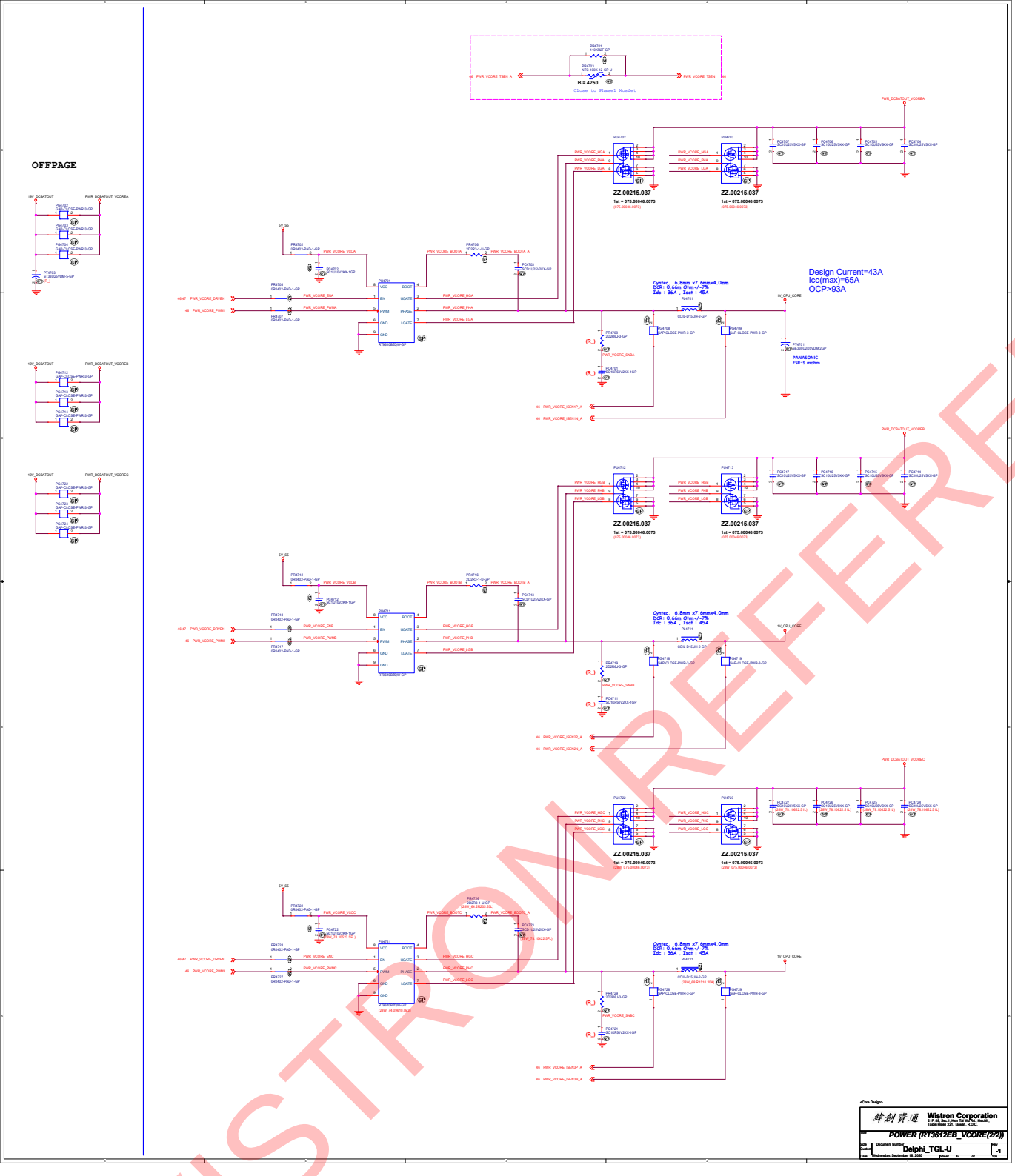
Title: POWER (RT3613EE_VCORE(1/2))
Size: Custom | Document Number: Delphi_TGL-U | Rev: -1
Date: Wednesday, September 16, 2020 | Sheet 46 of 105

WISTRON REFERENCE ONLY



WISTRON REFERENCE ONLY

Main Func = CPU_CORE

(Reserved)

WISTRON REFERENCE ONLY

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power_CSD97396_CPU_VCCGT

Size: A | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 48 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

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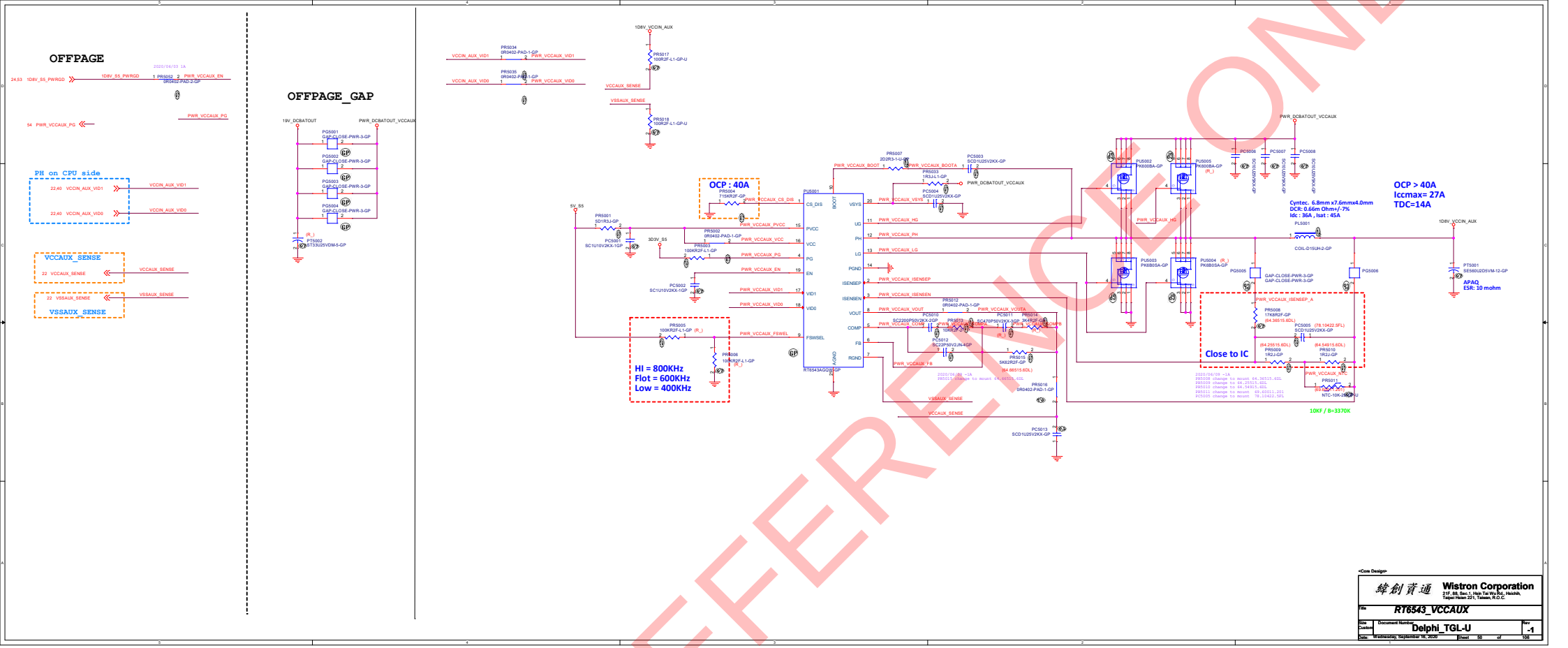
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
DC to DC_12V (SY8246)

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 49 of 106



WISTRON REFERENCE ONLY

OFFPAGE

S5

VDDQ_EN

S3

SE_VTT_EN

PH on EE Side

PWR_VDDQ_PG

OFFPAGE_GAP

19V_DCBATOUT

PWR_DCBATOUT_VDDQ

1D2V_S3

PWR_VDDQ

PWR_VDDQ_VLDOIN

0D6V_VREF_S0

PWR_VDDQVTT

VID

Table 1. VID and Reference Voltage Setting

VID	Reference Voltage (V)
High	0.675
Low	0.75

OCP setting

PWR_VDDQ_CS

PR5114 220KR2F-GP

PWR_VDDQ_VID

PWR_VDDQ_VDD

PR5109 0R0402-PAD-1-GP

PR5107 5D1R2F-GP

PC5102 SC1U10V2KX-1GP

PC5107 SC1U10V2KX-1GP

3D3V_S5

PR5111 10KR2J-3-GP

PWR_DCBATOUT_VDDQ

Freq. setting

750K -> 350K Hz

PR5113 750KR2F-GP

PU5101

PWR_VDDQ_PG

PWR_VDDQ_TON

PWR_VDDQ_EN

PWR_VTT_EN

PWR_VDDQ_VLDOIN

PC5109 SC10U6D3V3MX-GP

VTTGND

VTT

VTTSNS

RT8231AGQW-GP

PWR_VDDQ_BOOT

PWR_VDDQ_HG

PWR_VDDQ_PH

PWR_VDDQ_LG

PWR_VDDQ_VDDQ

PWR_VDDQ_FB

PWR_VDDQ_VTTREF

PC5116 SCD047U25V2KX-GP

Vout = 0.6V

Iomax = 0.75A

PC5106 SCD1U16V2KX-3GP

PC5118 SCD1U06D3V3MX-GP

PC5117 SCD1U06D3V3MX-GP

PR5112 2D2R3-1-UI-GP

PC5108 SCD1U25V2KX-GP

PU5102 PK600BA-GP

PU5103 PK680SA-GP

PC5103 SC4D7U25V6KX-GP

PC5104 SC4D7U25V6KX-GP

Close to output cap pin1, not inside of the output cap

PG5101 GAP-CLOSE-PWR-3-GP

PWR_VDDQ

Cyntec. 11.5mm x 10.3mm x 4.0 mm

DCR: 3~3.3mOhm

Idc : 18A , Isat: 36A

PL5101 COIL-1UH-97-GP

Icc(max)=11.5A

PC5113 SC22U06D3VMX-1GP

PC5110 SC22U06D3VMX-1GP

PC5111 SC22U06D3VMX-1GP

PC5112 SC22U06D3VMX-1GP

PC5114 SC22U06D3VMX-1GP

PC5119 SC22U06D3VMX-1GP

PC5120 SC22U06D3VMX-1GP

PC5121 SC22U06D3VMX-1GP

PC5122 SC22U06D3VMX-1GP

R1

PR5116 15K8R2F-GP

PC5115 SC18P50V2JN-1GP

R2

PR5117 20KR2F-L-GP

Vout Setting

Vout = Vref * (1 + R1/R2)

= 0.675 * (1 + 15.8K / 20K)

= 1.2V

VID vs Vref Table

VID Logic-High => Vref = 0.675 V

VID Logic-Low => Vref = 0.75 V

note. Vref can only be changed form 0.675v to 0.75v after power-on

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Enable

2D5V_S3_EN

PWR_2D5V_EN

Power Good

PH on EE Side

2D5V_S3_PWRGD

PWR_2D5V_PG

APL5934 for 2D5V

2D5V_S5

IMAX=0.3A

APL5934 need <1.8W

IMax=1.5A

PD=1.5A*(3.3V-2.5V)=1.2W

PWR_2D5V_VIN

PWR_2D5V_PG

PWR_2D5V_EN

PWR_2D5V_FB

PU5151 APL5934KAI-TRG-GP-U

PC5156 SC1U10V2KX-1GP

PC5151 SC10U06D3V3MX-GP

PR5151 100KR2J-1-GP

PC5155 SCD1U25V2KX-GP

PR5199 49K9R2F-L-GP

PG5156 GAP-CLOSE-PWR-3-GP

PC5153 SC10U06D3V3MX-GP

PC5154 SC10U06D3V3MX-GP

PC5152 SC68P50V2JN-1GP

R1

PR5152 21K5R2F-GP

R2

PR5153 10KR2F-2-GP

Vout = 0.8*(1+R1/R2)

=0.8*(1+21.5K/10K)

=2.52V

<Core Design>

Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8231_VDDQVTT; APL5934_VDDQVPP

Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 51 of 106

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Wistron Corporation
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Title: ***POWER (RSVD)***

Size	Document Number	Rev
A	Delphi_TGL-U	-1

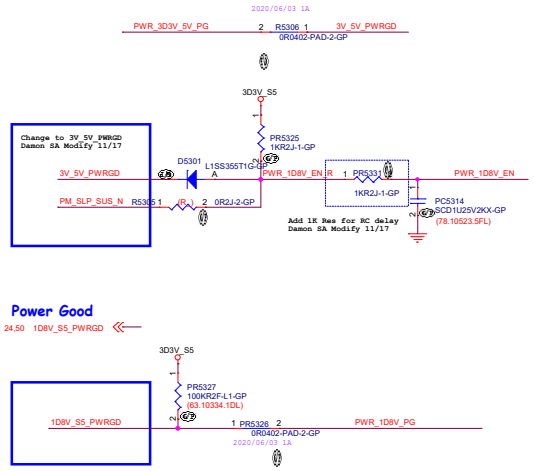
Date: Wednesday, September 16, 2020 Sheet 52 of 106

OFFPAGE

Enable

45 PWR_3D3V_5V_PG

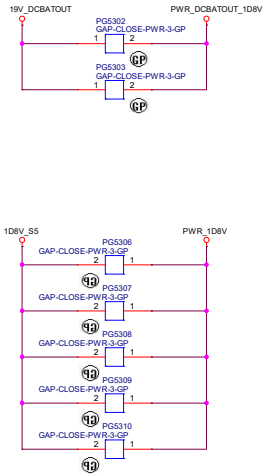
17,24,68 PM_SLP_SUS_N



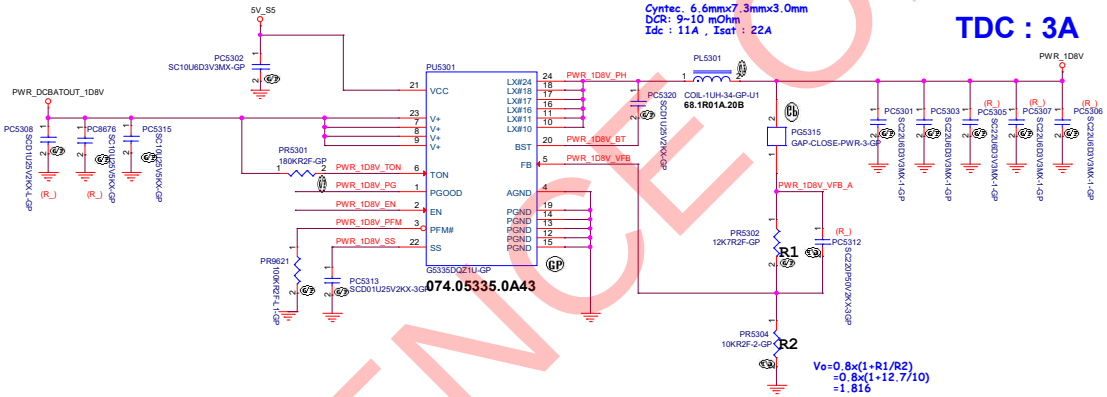
Power Good

24,50 1D8V_S5_PWRGD

OFFPAGE_GAP



G5335D for 1D8V



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RT8237C_1D8V
Size: Custom	Document Number: Delphi_TGL-U
Rev	-1
Date: Wednesday, September 16, 2020	Sheet 53 of 108

WISTRON REFERENCE ONLY

OFFPAGE

OFFPAGE_GAP

EE Side

EE Side

Power Good Not use

PWR_12V

Input ripple current =0.5828A
10uF/25V, Ripple Current =1000mA
Input capacitance = 20uF

MAG. 7.6mm*6.8mm*3mm
DCR: 68 mOhm
Idc : 4A , Isat : 5.5A

IMAX=1A,OCP>10A
PWM Frequency=340kHz
L2R=1.41A/2A=141.2%
10uF/25V, Ripple Current=1Arms
Cout capacitance=60uF

Vout Setting
Vout = Vref * (1 + (R1/R2))
= 0.8 * (1 + (71.5K / 5.1K))
= 12.015V

OFFPAGE

VNN Enable

1D05V Enable

1D05V Power Good

PH on EE Side

OFFPAGE-GAP

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

Murata.
2.7mm×2.2mmX1.2mm
DCR: 59m Ohm
Idc : 3A , Isat : 3A

Murata.
2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A , Isat : 1A

Design Current=0.2A
OCP>0.8A

Design Current=0.2A
OCP>0.8A

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Taipei Hsien 221, Taiwan, R.O.C.

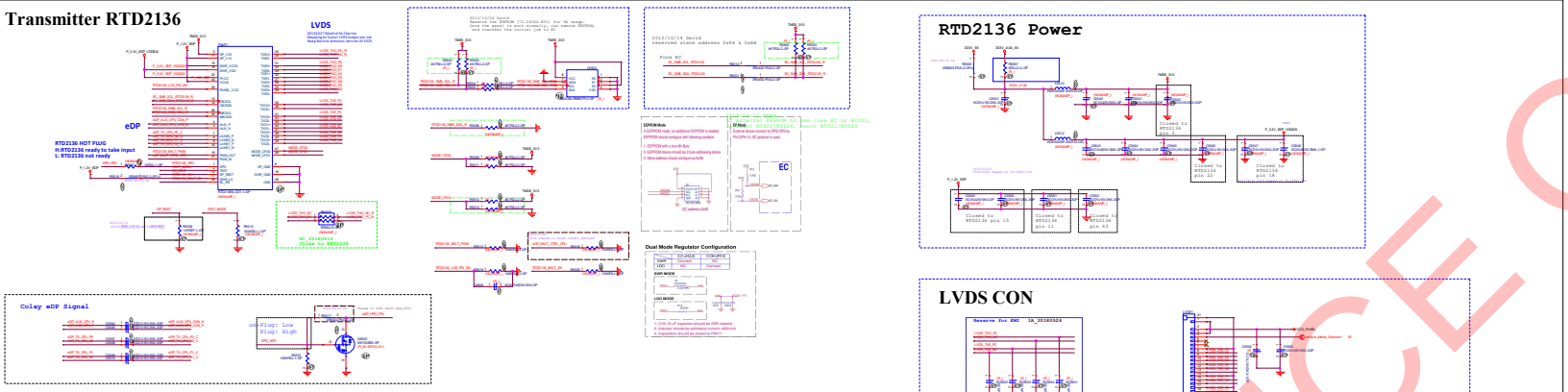
Title: RT8130B_12V;APW8738_ByPASS

Size: D | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 54 of 108

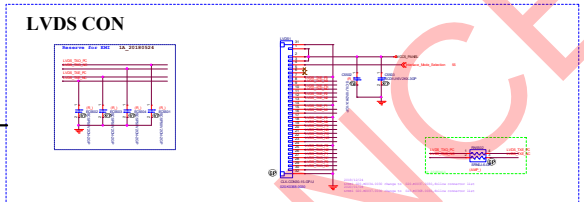
WISTRON REFERENCE ONLY

Transmitter RTD2136

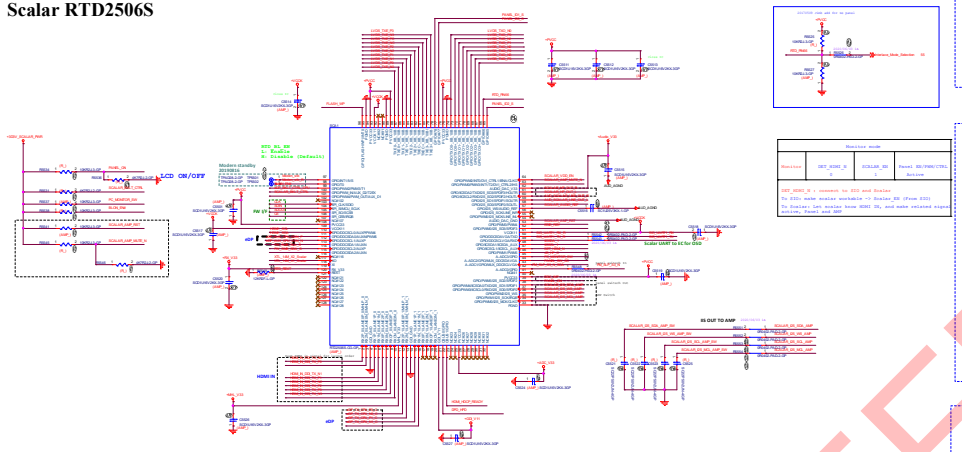


RTD2136 Power

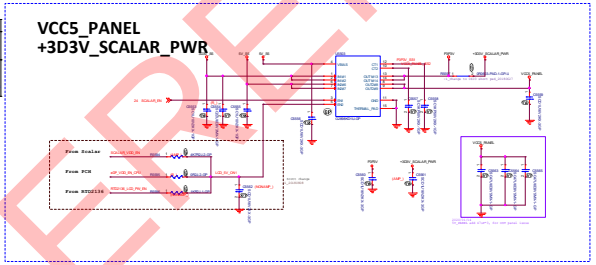
LVDS CON



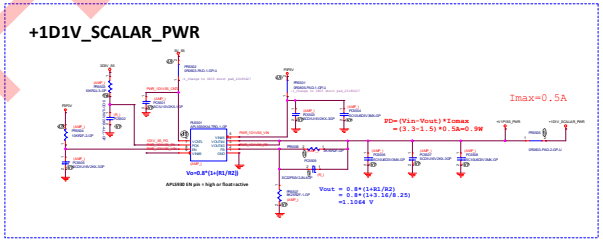
Scalar RTD2506S

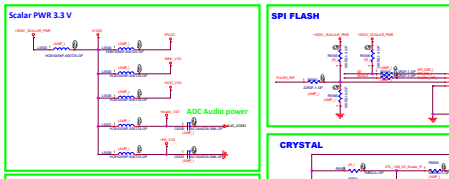


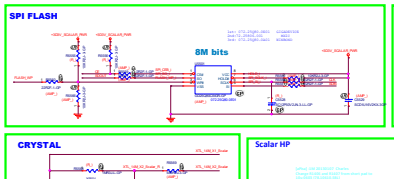
VCC5_PANEL
+3D3V_SCALAR_PWR

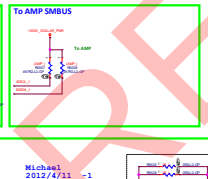


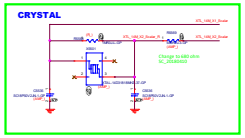
+1D1V_SCALAR_PWR

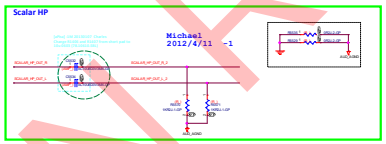


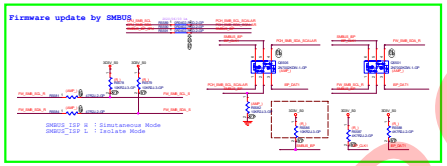


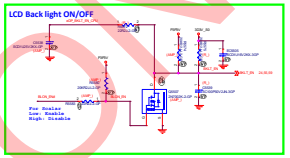


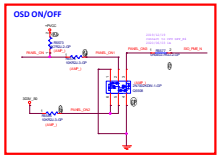


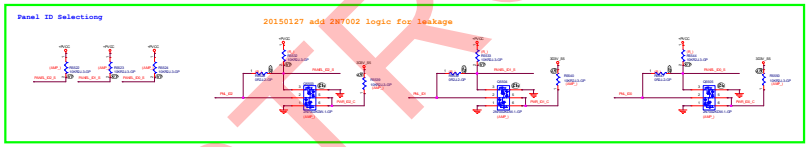












Scalar Spec Table

GPI input		From	High	Low	Default
Pin69	GPI-1 PC Power ON PM_SLP_S3_N	SB	PC	Monitor	Monitor
Pin109	GPI-2 Mode change/ Panel On/Off	SW	Normal	Touch	PC: PC (PC->HDMI) Monitor: HDMI, VGA (HDMI)

GPO output

Pin55	GPO-2 Panel On/OFF SCALAR_VDD_EN	Scalar	ON	OFF	PC: ON Monitor: Detect Signal
Pin104	GPO-3 PC/Monitor PC_MONITOR_SW	Scalar	PC	Monitor	PC: PC, Monitor: HDMI, VGA
Pin99	GPO-5 Video BLON_EN_N	Scalar	Disable	Enable	Disable
Pin72	GPO-6 Audio Mute	Scalar	on-Mute	MUTE	MUTE

WISTRON CONFIDENCE ONLY

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Display (RSVD)*

Size	Document Number	Rev
A	Delphi_TGL-U	-1

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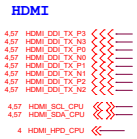
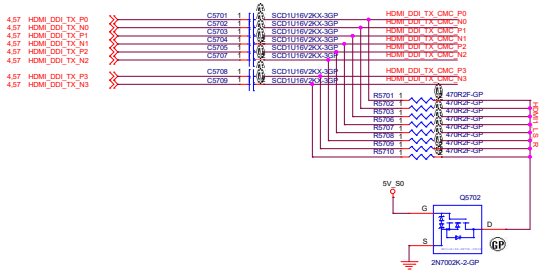
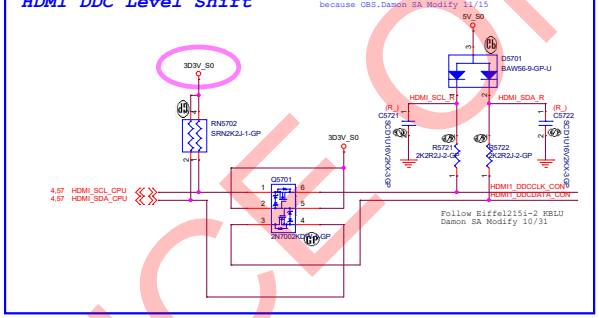
HDMI V1.4b

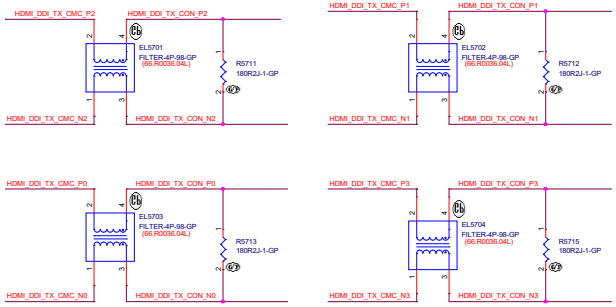


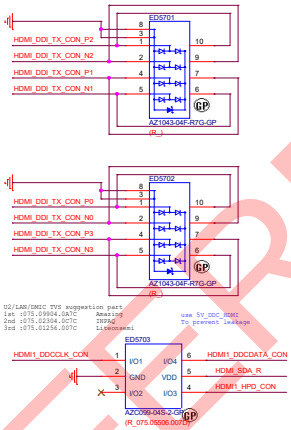


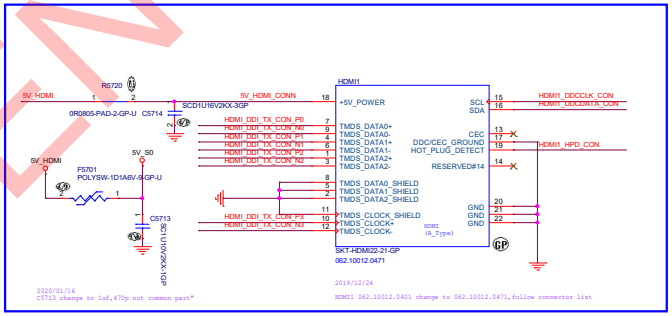
HDMI DDC Level Shift

D5701 change from 75.00056.07D to 75.00056.07D, because OBS.DamoN SA Modify 11/15

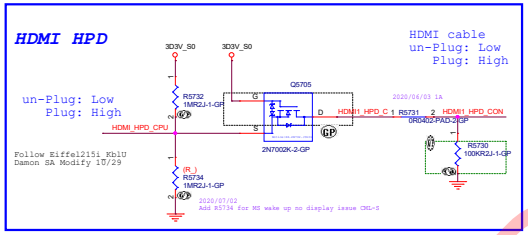








HDMI HPD



WISTRON REFERENCE ONLY

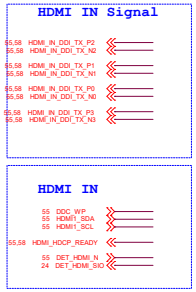
<Core Design>

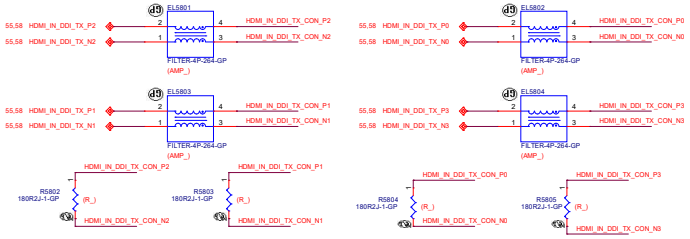
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

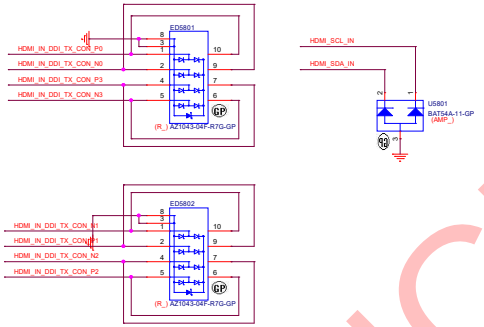
Title: Display (HDMI/Conn)

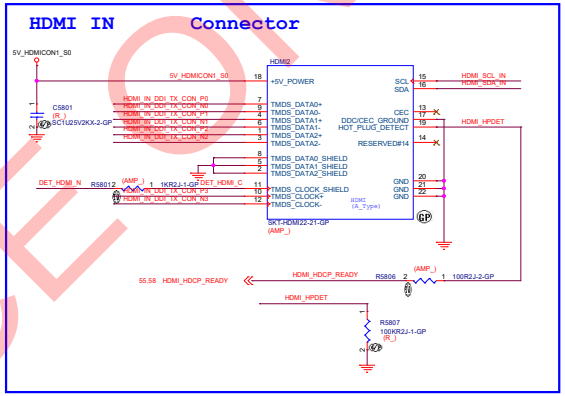
Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

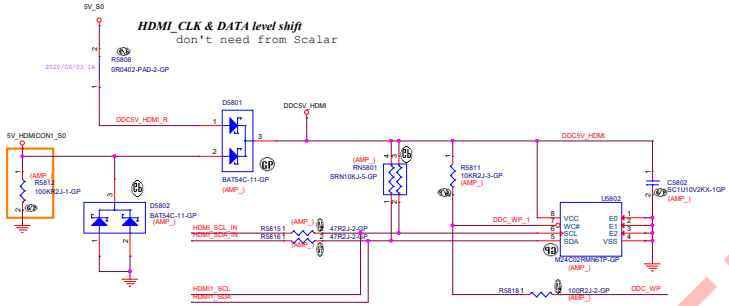
Date: Wednesday, September 16, 2020 | Sheet 57 of 106

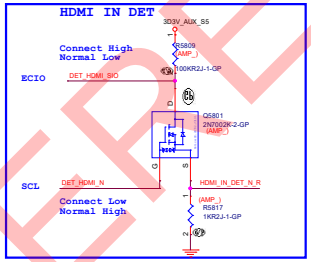


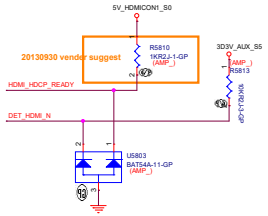












WISTRON REFERENCE ONLY

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (RSVD) DP / DVI

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LVDS Converter

SMBUS

24 EC_SMB_SCL_OZ
24 EC_SMB_SDA_OZ

Back light control

4,55 eDP_BKLT_EN_CPU
4,55 eDP_BKLT_CTRL_CPU

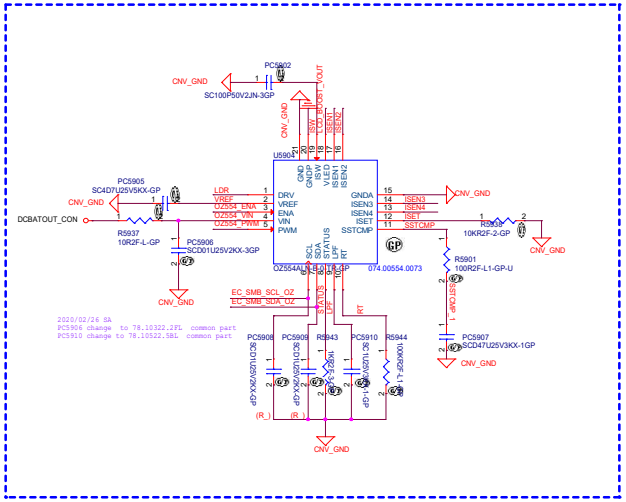
RTD2136

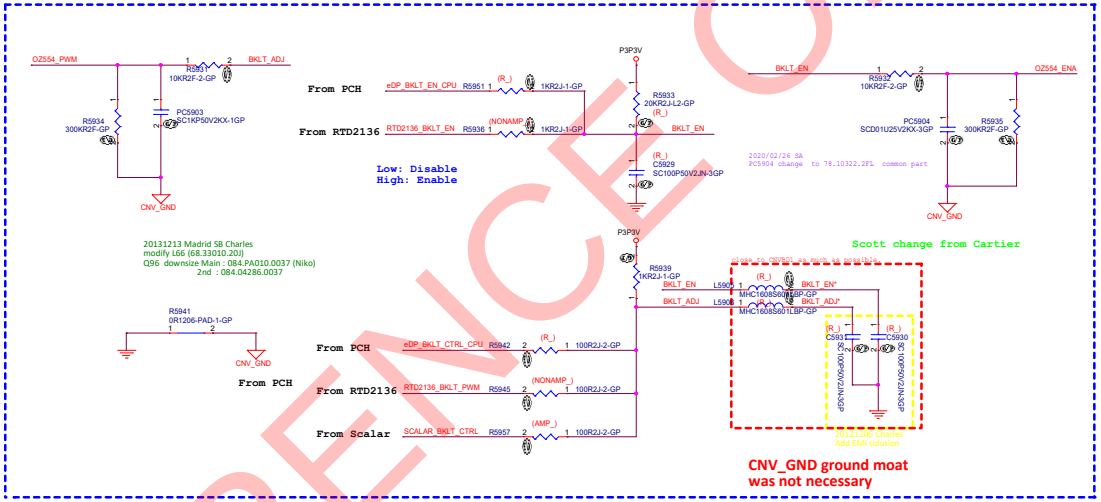
55 RTD2136_BKLT_EN
55 RTD2136_BKLT_PWM

24,55 BKLT_EN
55 SCALAR_BKLT_CTRL

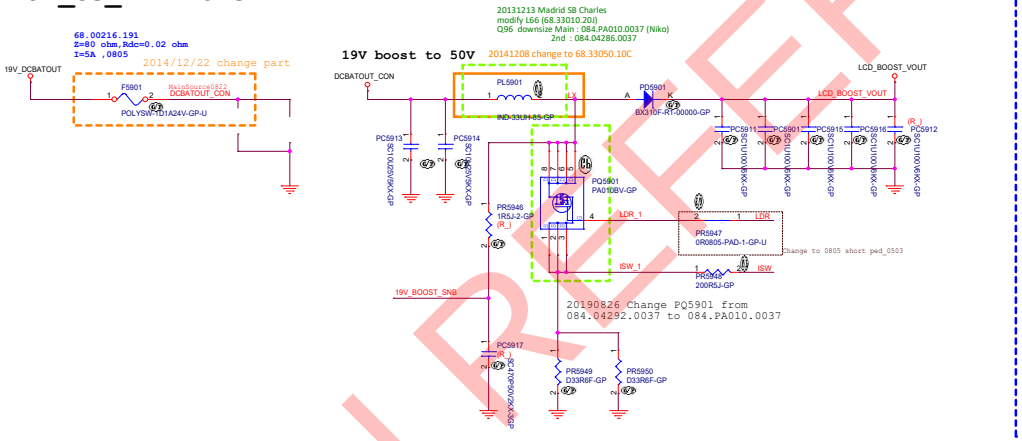
Panel ID

24,55 PNL_ID2
24,55 PNL_ID1
24,55 PNL_ID0

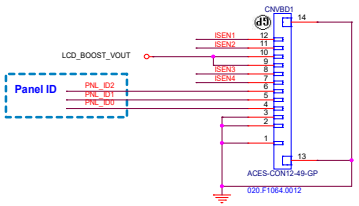




+19V_S5_INV Power



Converter Conn



<Core Design>

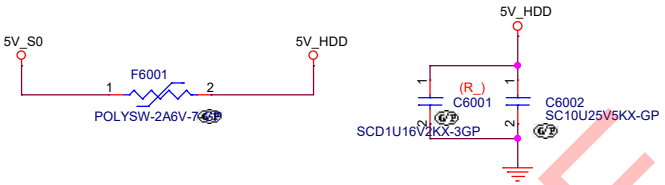
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (RSVD) Backlight PW
Size: Custom | Document Number: Delphi_TGL-U | Rev: -1
Date: Wednesday, September 16, 2020 | Sheet 59 of 106

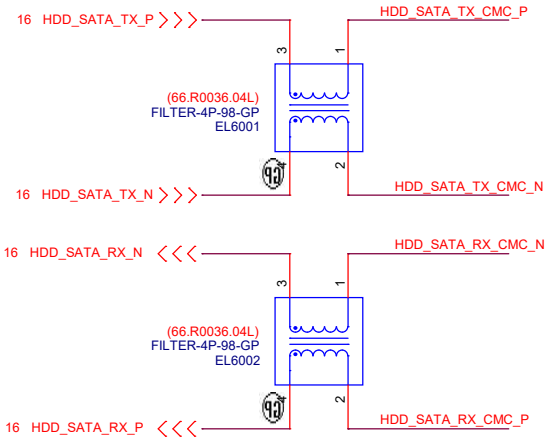
WISTRON REFERENCE ONLY

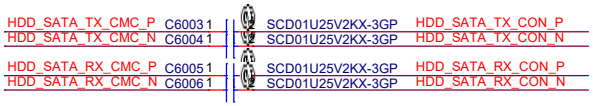
SATA HDD Connector

Layout: Put them together

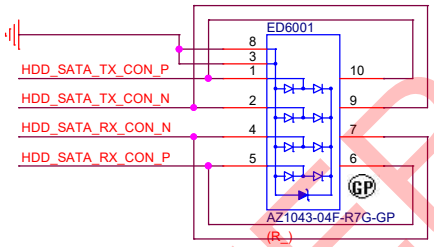


close to connector

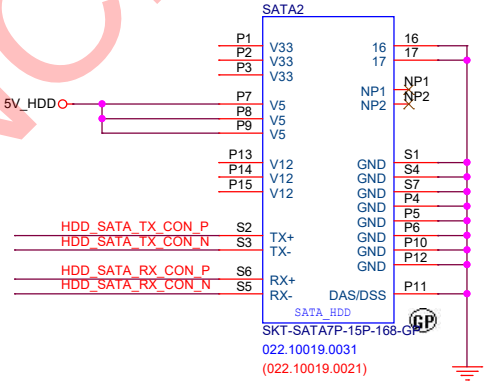




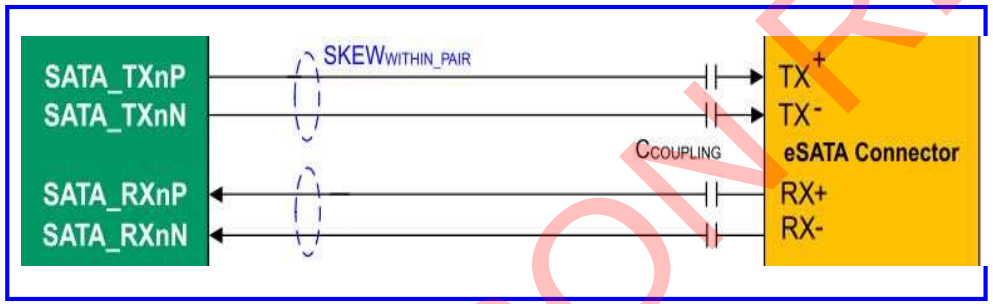
2020/02/26 SA
C6003,C6004,C6005,C6006 change to 78.10322.2FL common part



HDD CONN



2020/01/08
SATA1change from 022.10019.0021 to 022.10019.0031



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

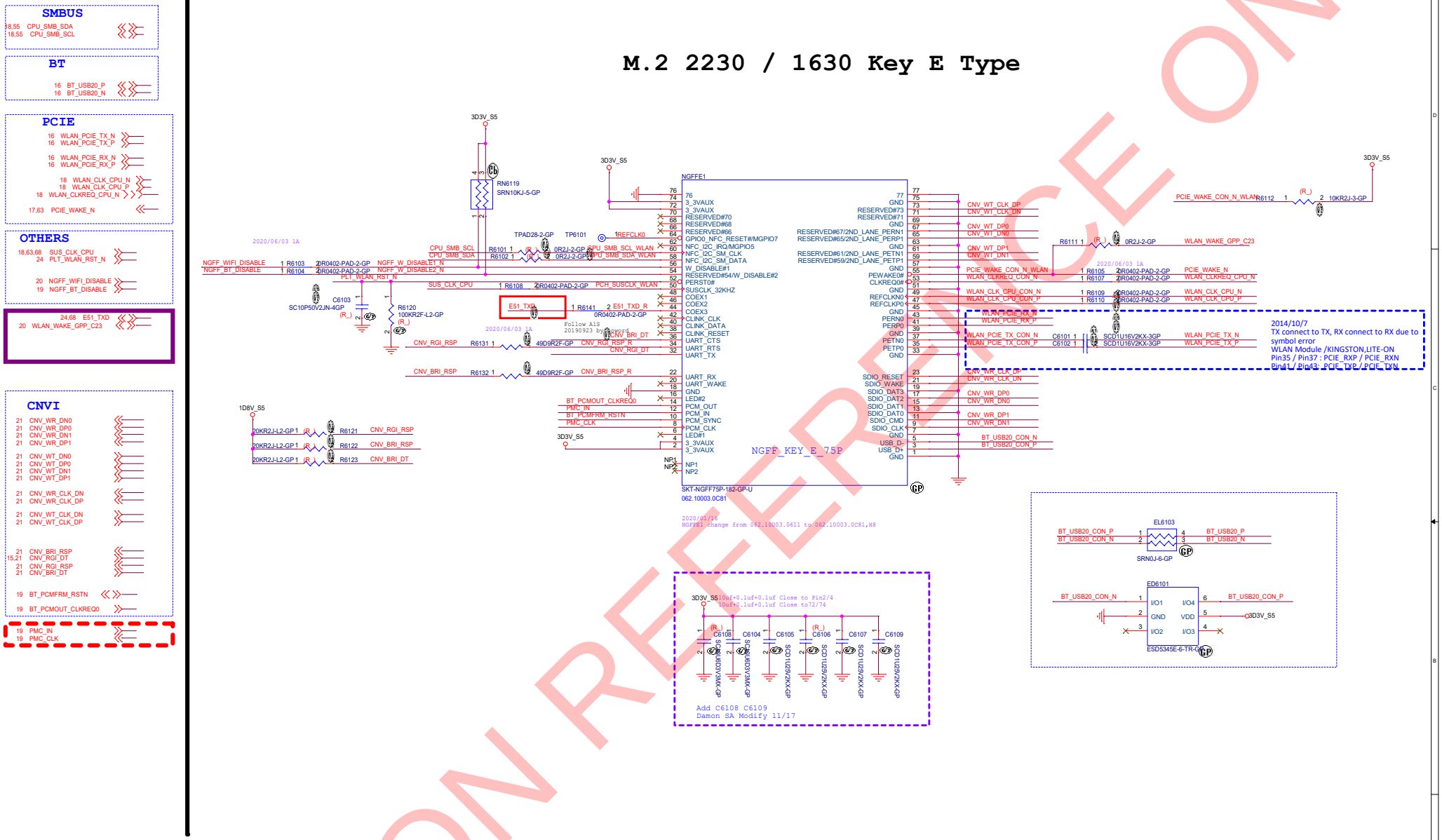
Title: ***INT IO (HDD)***

Size	Document Number	Rev
B	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 60 of 106

WISTRON REFERENCE ONLY

M.2 2230 / 1630 Key E Type



WISTRON REFERENCE ONLY

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (HDD)

Size: C | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 61 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD) WWAN*

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 62 of 106

M.2 SSD

HPGP_M2_SATA_DET#	Module Type
0	SSD-SATA
1	SSD-PCIE

M.2 Key M Type

16 SSD_PCIE_TX_P0
16 SSD_PCIE_TX_N0
16 SSD_PCIE_RX_P0
16 SSD_PCIE_RX_N0
16 SSD_PCIE_TX_P1
16 SSD_PCIE_TX_N1
16 SSD_PCIE_RX_P1
16 SSD_PCIE_RX_N1
16 SSD_PCIE_TX_P2
16 SSD_PCIE_TX_N2
16 SSD_PCIE_RX_P2
16 SSD_PCIE_RX_N2
16 SSD_PCIE_TX_P3
16 SSD_PCIE_TX_N3
16 SSD_PCIE_RX_P3
16 SSD_PCIE_RX_N3

SSD CLK

18 SSD_CLK_CPU_N
18 SSD_CLK_CPU_P
18 SSD_CLKREQ_CPU_N
17,61 PCIE_WAKE_N
16 M2_PEDET1
16 M2_DEVSLP1
8,51,68 SUS_CLK_CPU
24 PLTRST_SSD

SATA

16 SSD_SATA_TX_P
16 SSD_SATA_TX_N
16 SSD_SATA_RX_P
16 SSD_SATA_RX_N

3D3V_S5
R6310 1 (R_) 2 10KR2J-3-GP PCIE_WAKE_CON_N_SSD

3D3V_S0
HPGP_M2_SATA_DET_N R6305 1 2 10KR2J-3-GP

2019/12/24
NGFFM1 062.10003.0E81 change to 062.10003.0D71,follow connector list
2020/01/08
NGFFM1 062.10003.0D71 change to 062.10003.0E81 ,follow connector list

NGFFM1
SUS_CLK_CPU R6311 1 33R2J-2-GP SUSCLK_SSD
PCIE_WAKE_N R6301 1 (R_) 2 0R2J-2-GP PCIE_WAKE_CON_N_SSD
SSD_CLKREQ_CPU_N 1 R6302 2 0R402-PAD-2-GP SSD_CLKREQ_N_CON
PLTRST_SSD 1 R6303 2 0R402-PAD-2-GP PLT_RST_N_SSD
M2_DEVSLP1 R6323 1 (R_) 0R2J-2-GP M2_DEVSLP1_CON

H:PCIE
L:SATA

2020/06/03 1A
1 R6306 2 0R402-PAD-2-GP M2_PEDET1
(R_) 1 R6308 2 10KR2J-3-GP

2020/06/03 1A
SSD_CLK_CPU_CON_P 1 R6313 2 0R402-PAD-2-GP SSD_CLK_CPU_P
SSD_CLK_CPU_CON_N 1 R6314 2 0R402-PAD-2-GP SSD_CLK_CPU_N

SSD_PCIE_TX_CON_P0
SSD_PCIE_TX_CON_N0
SSD_PCIE_RX_CON_N0
SSD_PCIE_RX_CON_P0

SSD_PCIE_TX_CON_P1 C6308 1 SCD22U10V2KX-1GP SSD_PCIE_TX_P1
SSD_PCIE_TX_CON_N1 C6309 1 SCD22U10V2KX-1GP SSD_PCIE_TX_N1
SSD_PCIE_RX_P1
SSD_PCIE_RX_N1
SSD_PCIE_TX_CON_P2 C6310 1 SCD22U10V2KX-1GP SSD_PCIE_TX_P2
SSD_PCIE_TX_CON_N2 C6311 1 SCD22U10V2KX-1GP SSD_PCIE_TX_N2
SSD_PCIE_RX_P2
SSD_PCIE_RX_N2
SSD_PCIE_TX_CON_P3 C6331 1 SCD22U10V2KX-1GP SSD_PCIE_TX_P3
SSD_PCIE_TX_CON_N3 C6332 1 SCD22U10V2KX-1GP SSD_PCIE_TX_N3
SSD_PCIE_RX_P3
SSD_PCIE_RX_N3

SKT-NGFF75P-217-GP

PLT_RST_N_SSD
(R_) C6301 SC1U10V2KX-GP
RSVD for EMI
PLT_RST_N_SSD
D6301 AZ5725-01FDR7G-GP (R_)

CLOSE TO PINS 1,6,10
C6305 SCD1U16V2KX-3GP
C6303 SCD1U16V2KX-3GP
C6341 SCD1U16V2KX-3GP
C6342 SC10U6D3V3MX-GP

U6304
SSD_PCIE_RX_CON_P0 C6312 1 SCD22U10V2KX-1GP SSD_PCIE_RX_SW_P0
SSD_PCIE_RX_CON_N0 C6313 1 SCD22U10V2KX-1GP SSD_PCIE_RX_SW_N0
SSD_PCIE_TX_CON_P0 R6332 2 0R402-PAD-2-GP SSD_PCIE_TX_SW_P0
SSD_PCIE_TX_CON_N0 R6322 2 0R402-PAD-2-GP SSD_PCIE_TX_SW_N0
HPGP_M2_SATA_DET_N
PI3PCIE3212ZBE-DAX-GP-U

2020/06/03 1A
SSD_SATA_RX_C_P R6315 2 0R402-PAD-2-GP SSD_SATA_RX_P
SSD_SATA_RX_C_N R6316 2 0R402-PAD-2-GP SSD_SATA_RX_N
SSD_SATA_TX_C_P C6012 1 SCD01U25V2KX-3GP SSD_SATA_TX_P
SSD_SATA_TX_C_N C6013 SCD01U25V2KX-3GP SSD_SATA_TX_N
SSD_PCIE_RX_C_P0 R6317 2 0R402-PAD-2-GP SSD_PCIE_RX_P0
SSD_PCIE_RX_C_N0 R6318 2 0R402-PAD-2-GP SSD_PCIE_RX_N0
SSD_PCIE_TX_C_P0 C6306 1 SCD22U10V2KX-1GP SSD_PCIE_TX_P0
SSD_PCIE_TX_C_N0 C6307 SCD22U10V2KX-1GP SSD_PCIE_TX_N0

2019/12/27
add SATA/PCIE switch circuit follow Petra238
2020/01/17
R6319/6320 change to 0.22uf cap, vendor suggestion

2020/02/26 SA
C6012,C6013 change to 78.10322.2FL common part

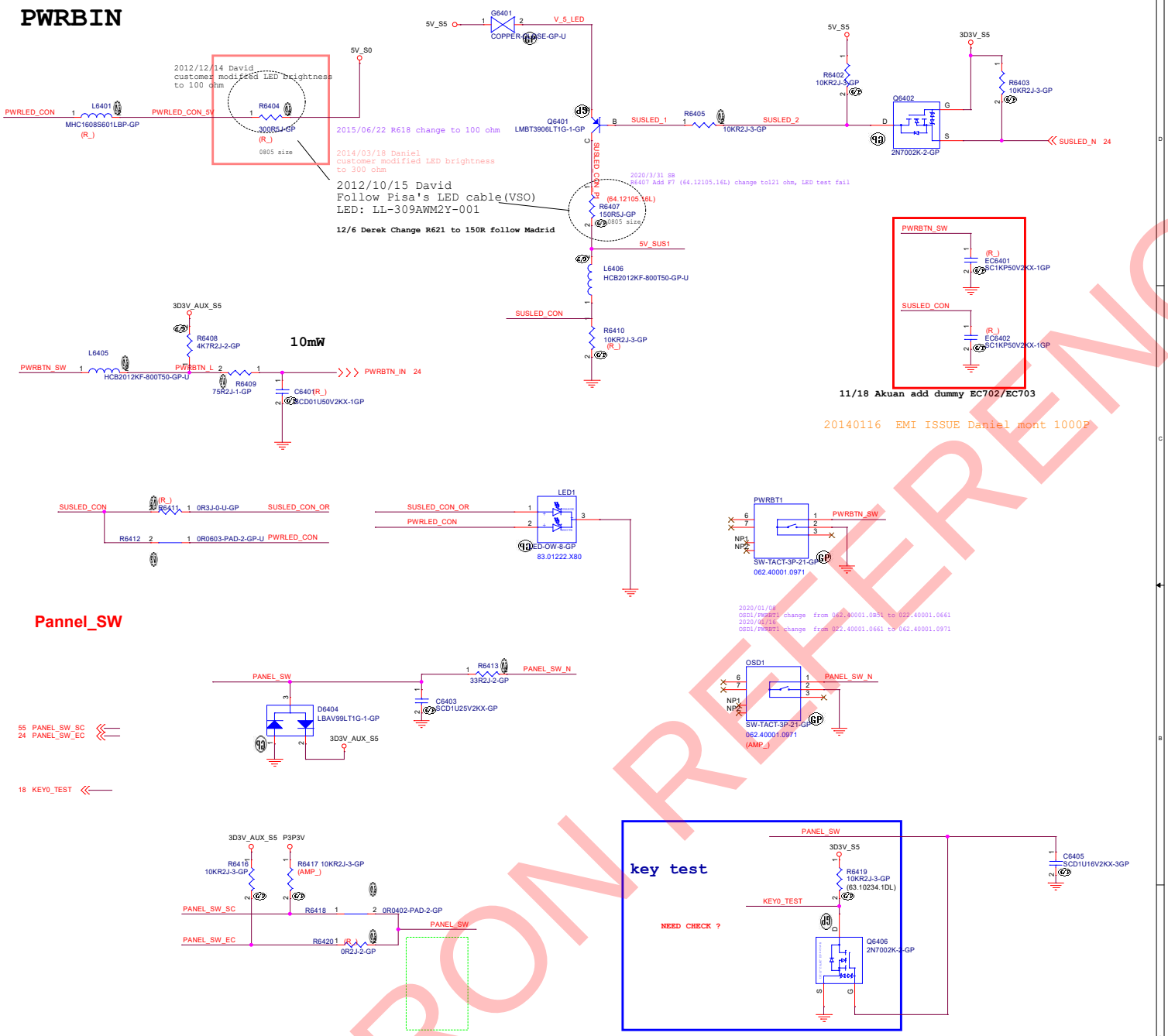
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD-NGFF-1)
Size: Custom | Document Number: Delphi_TGL-U | Rev: -1
Date: Wednesday, September 16, 2020 | Sheet 63 of 106

WISTRON REFERENCE ONLY

PWRBIN



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED / Button / Power Button		
Size: Custom	Document Number: Delphi_TGL-U	Rev: -1
Date: Wednesday, September 16, 2020	Sheet 64 of 106	

WISTRON REFERENCE ONLY

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
INT IO (Key BoardTouch Pad)

Size	Document Number	Rev
A	Delphi_TGL-U	-1

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***066_IO Board Conn (RSVD)***

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 66 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

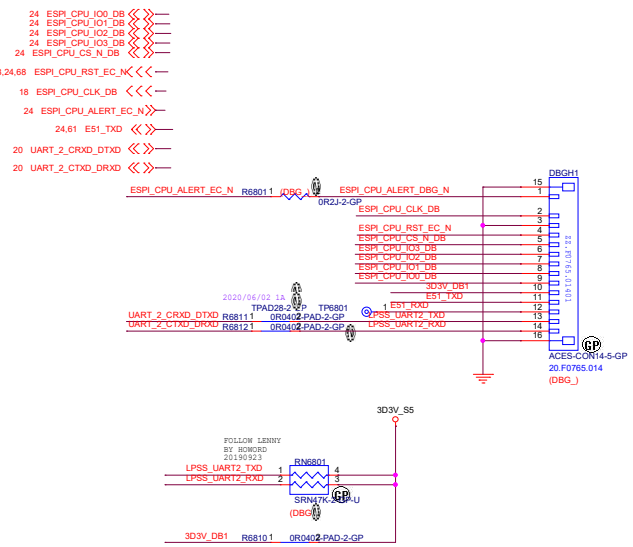
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 067_Sensor (Hall Sensor/Vol BOT

Size: A | Document Number: Delphi_TGL-U | Rev: -1

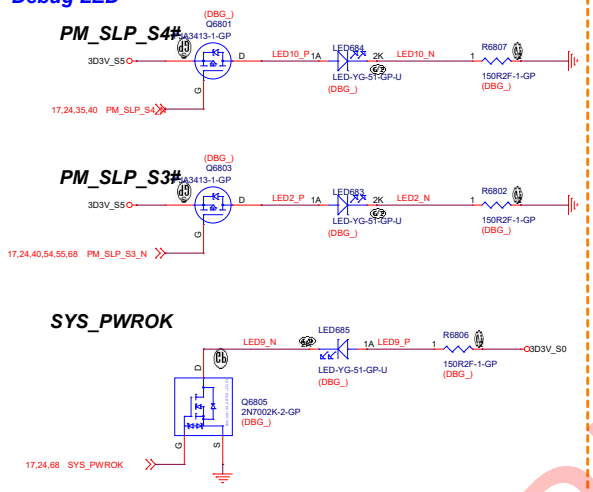
Date: Wednesday, September 16, 2020 | Sheet 67 of 106

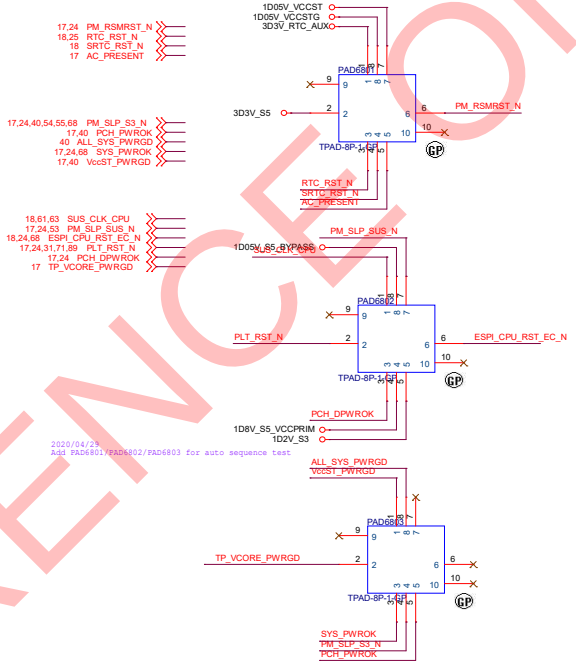
eSPI DEBUG PORT



Add Debug Led,follow Mocha.
Damon SA Modify 11/17

Debug LED





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Debug (LPC debug)**

Size	Document Number	Rev
Custom	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 68 of 106

WISTRON REFERENCE ONLY

(Reserved)

WISTRON REFERENCE ONLY

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緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***069_Sensor (RSVD) (GYROSCOPE)***

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 69 of 106

(Reserved)

WISTRON REFERENCE ONLY

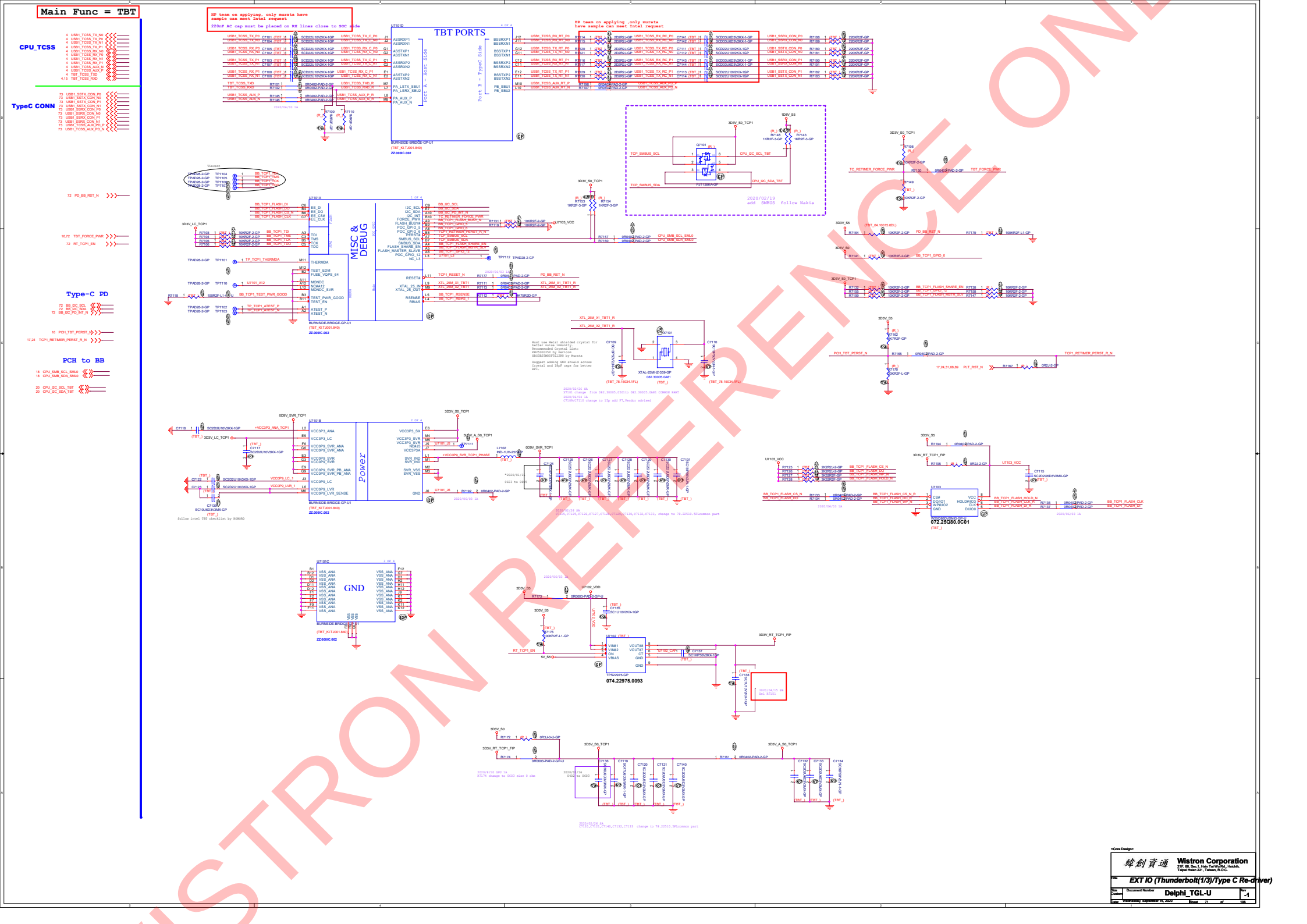
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
070_Sensor (RSVD)

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 70 of 106


Main Func = TBT
CPU_TCSS
TypeC CONN
Type-C PD
PCH to BB
TBT PORTS
MISC & DEBUG
Power
GND
HP team on applying, only murata have sample can meet Intel request
220nF AC cap must be placed on RX lines close to SOC side
Port A - Host Side
Port B - TypeC Side
Must use Metal shielded crystal for better noise immunity.
Recommended Crystal List:
FK255002252 by Pericom
SX3S27M033F2L1X0 by Murata
Suggest adding GND shield across Crystal and 18pF caps for better EFI.
follow Intel TBT checklist by HOWORD
2020/02/19
add SMBUS follow Nakia
074.22975.0093
072.25Q80.0C01
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
EXT IO (Thunderbolt(1/3)/Type C Re-driver)
Delphi_TGL-U
Rev -1
Wednesday, September 16, 2020
Sheet 21 of 106

Main Func = TypeC

PD to EC/TP

24 UPD1_SMBINT_N
24 EC_SMB_SDA_PD
24 EC_SMB_SCL_PD

PD To PCH

17 TBT_PD_ALERT_N

PD To BB

71 BB_I2C_SCL
71 BB_I2C_SDA
71 BB_I2C_PD_INT_N
71 PD_BB_RST_N
16,71 TBT_FORCE_PWR
71 RT_TCP1_EN
18 CPU_SMB_SCL_SML1
18 CPU_SMB_SDA_SML1
73 USB1_CON_CC1
73 USB1_CON_CC2

GPIO	Pin #	Package Pin Name	TPS65992D		
			TGL w/ Burnside Bridge RT	RKL w/o TBT	RKL w/ TR or MR
0	5	GPIO0	RT_FORCE_PWR	-	-
1	6	GPIO1 (HPD_Tx)	RT_EN	HPD_Tx	-
2	7	GPIO2 (PROCHOT#)	PROCHOT#	PROCHOT#	PROCHOT#
3	19	GPIO3	RT_RST	-	TBT_RST
4	26	GPIO4 (USB_P)	DDM_MUX_FLIP*	DDM_MUX_FLIP*	DDM_MUX_FLIP*
5	27	GPIO5 (USB_N)	DDM_MUX_EN*	DDM_MUX_EN*	DDM_MUX_EN*
6	36	GPIO6	-	-	-
7	37	GPIO7	EN_PD_HV_1	EN_PD_HV_1	EN_PD_HV_1

PD to EC

PD To PCH

PD To BB

Default setting:0x50

Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1)			Without using R_{UP} or R_{DOWN}	ADCINx decoded value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: (Thunderbolt(2/3)/Type C CC Logic)

Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 72 of 106

Main Func = TBT

71 USB1_SSTX_CON_P0
71 USB1_SSTX_CON_N0
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N1

71 USB1_SSRX_CON_P0
71 USB1_SSRX_CON_N0
71 USB1_SSRX_CON_P1
71 USB1_SSRX_CON_N1

71 USB1_TCSS_AUX_PD_P
71 USB1_TCSS_AUX_PD_N

72 USB1_CON_CC1
72 USB1_CON_CC2

16 USB3_USB20_P
16 USB3_USB20_N

USB3_USB20_P — EL7301 — USB3_USB20_CON_P
USB3_USB20_N — EL7301 — USB3_USB20_CON_N
DUMMY-FILTER-4P-132-GP
(TBT_068.09002.2001)

20V_VCCPD_VBUS
(TBT_) C7320 SCD1U25V2KX-GP

USCR1
SKT-USB30-29-GP
062.10009.0A51
(TBT_)

A1 GND	GND B1		
A2 SSTXP1	SSTXP2 B2	USB1_SSTX_CON_P1	USB1_SSTX_CON_P0
A3 SSTXN1	SSTXN2 B3	USB1_SSTX_CON_N1	USB1_SSTX_CON_N0
A4 VBUS#A4	VBUS#B4 B4		
A5 CC1	CC2 B5	USB1_CON_CC2	USB1_CON_CC1
A6 DP1	DP2 B6	USB3_USB20_CON_P	USB3_USB20_CON_P
A7 DN1	DN2 B7	USB3_USB20_CON_N	USB3_USB20_CON_N
A8 RFU1	RFU2 B8	USB1_TCSS_AUX_PD_N	USB1_TCSS_AUX_PD_P
A9 VBUS#A9	VBUS#B9 B9		
A10 SSRXN2	SSRXN1 B10	USB1_SSRX_CON_N0	USB1_SSRX_CON_N1
A11 SSRXP2	SSRXP1 B11	USB1_SSRX_CON_P0	USB1_SSRX_CON_P1
A12 GND	GND B12		
	CHASSIS#13 13		
	CHASSIS#14 14		
	CHASSIS#15 15		
	CHASSIS#16 16		
	CHASSIS#17 17		
	CHASSIS#18 18		

C7321 (R_) SC100P50V1JN-GP
C7322 (R_) SC100P50V1JN-GP

20V_VCCPD_VBUS
(TBT_) C7301 SCD1U25V2KX-GP
(TBT_) C7302 SCD1U25V2KX-GP
(TBT_) C7303 SCD1U25V2KX-GP
(TBT_) C7304 SCD1U25V2KX-GP

Close to pin A4, B4, A9, B9

USB1_SSRX_CON_P0 — ED7302 PESD5V0H1BSFYL-GP-U1 — (TBT_)
USB1_SSRX_CON_N0 — ED7303 PESD5V0H1BSFYL-GP-U1 — (TBT_)
USB1_SSRX_CON_P1 — ED7304 PESD5V0H1BSFYL-GP-U1 — (TBT_)
USB1_SSRX_CON_N1 — ED7305 PESD5V0H1BSFYL-GP-U1 — (TBT_)

USB1_SSTX_CON_P0 — ED7301 PESD5V0H1BSFYL-GP-U1 — (TBT_)
USB1_SSTX_CON_N0 — ED7306 PESD5V0H1BSFYL-GP-U1 — (TBT_)
USB1_SSTX_CON_P1 — ED7315 PESD5V0H1BSFYL-GP-U1 — (TBT_)
USB1_SSTX_CON_N1 — ED7316 PESD5V0H1BSFYL-GP-U1 — (TBT_)

USB3_USB20_CON_P — ED7309 PESD5V0H1BSFYL-GP-U1 — (TBT_)
USB3_USB20_CON_N — ED7310 PESD5V0H1BSFYL-GP-U1 — (TBT_)

2020/01/06
Need check TVS PART

USB1_CON_CC1 — ED7317 PESD5V0H1BSFYL-GP-U1 — (TBT_)
USB1_CON_CC2 — ED7312 PESD5V0H1BSFYL-GP-U1 — (TBT_)
USB1_TCSS_AUX_PD_P — ED7313 PESD5V0H1BSFYL-GP-U1 — (TBT_)
USB1_TCSS_AUX_PD_N — ED7314 PESD5V0H1BSFYL-GP-U1 — (TBT_)

2020/04/30
Del ED7311/ED7318

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Thunderbolt(3/3)/Type C Conn)
Size: C
Document Number: Delphi_TGL-U
Rev: -1
Date: Wednesday, September 16, 2020
Sheet 73 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *074_EXT IO (RSVD)*

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 74 of 106

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Taipei Hsien 221, Taiwan, R.O.C.

Title	*075_EXT IO (RSVD)*	
Size A	Document Number **Delphi_TGL-U**	Rev **-1**
Date: Wednesday, September 16, 2020	Sheet 75 of 106	

WISTRON REFERENCE ONLY

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU(1/5) PEG

Size: Custom | Document Number: =Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 78 of 106

WISTRON REFERENCE ONLY

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU(2/5)DIGITALOUT

Size	Document Number	Rev
C	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 77 of 106

WISTRON REFERENCE ONLY

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU(3/5):VRAM I/F

Size: C | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 78 of 106

WISTRON REFERENCE ONLY

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd.
Hsichih, Taipei Hsien

COPLUS-EQ-CIPCKSTRAP

Document Number
Project_102_2

Wednesday, September 19, 2012 Sheet 1 of 1

WISTRON REFERENCE ONLY

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1 Hsin Tai Wu Rd
Hsichih, Taipei Hsien

File: GPU(5/5):PWR/GND

Size: Custom | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 88 of 106

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GDDR6_VRAM1,2***

Size	Document Number	Rev
Custom	Delphi_TGL-U	-1
Date: Wednesday, September 16, 2020	Sheet 81 of 106	

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GDDR6_VRAM POWER

Size	Document Number	Rev
A2	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 82 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VRAM 5,6 (2/4)

Size: A | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 83 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VRAM 7,8 (2/4)

Size: A | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 84 of 106

WISTRON REFERENCE ONLY

•Core Design•

wistron

Wistron Incorporated
21F, 88, Sec. 1 Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: RT8816_VGACORE

Size: Custom | Document Number: Dalphi_TGL-U | Rev: V.4

Date: Wednesday, September 16, 2020 | Sheet 60 of 100

WISTRON REFERENCE ONLY

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU Switch

Size: A | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 87 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU Switch

Size: A | Document Number: Delphi_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 88 of 106

WLAN (M2 key E)

HS2
STF256R113-UH286-1-GP

2020/01/08
Del SSD HS2/HS3

2020/01/08
WLAN change to HS2 and chagne to 334.08002.0001

Battery Symbol

BATT1
BATTERY CR2032
(23.20068.001)

23.20068.001
KTS
BBBCR2032BX
23.22063.001 JHT
CR2032 JHT

23.21012.001
KTS
BBBCR2032BN

Scre Hole (PCB New type MOUNTING HOLES)

H1 H2 H3 H5 H7

GEN315R158-8-F-C-S-GP-U
ZZ.SCREW.541

For 238i

LABEL

LBL1
LABEL
(40.3BZ23.011)

MB serial NO# and MAC address
40.3BZ24.011 -> 30 x 15mm
40.3KP03.011 -> 35 x 15mm
45.41101.011 -> 35 x 15mm
45.41107.021 -> 70 x 8mm
40.3BZ23.011 -> 30 x 10mm
40.3BZ24.011 -> 30 x 15mm
CARD
45.ACA01.0C1 -> 32 x 7mm
MIC CARD
345.02801.0001 -> 12 x 6mm

215i
Part Number | Manufacture (Gerber Out) SA
Q48.Y0000.0QHA | CEE (Yes)
Q48.Y0000.0RBA | GLOBALBRAN
Q48.Y0000.0QGA | HANNSTAR (Yes)

215i
Part Number | Manufacture (Gerber Out) SB
348.0EE07.00SB | GLOBALBRAN
348.0EE06.00SB | HANNSTAR (Yes)

215i -1
Part Number | Manufacture (Gerber Out) -1
348.0EE07.0011 | GLOBALBRAN
348.0EE06.0011 | HANNSTAR (Yes)

HeatSink Symbol

CPUHS1
HEATSINK
(P_360.06R02.0011)

2016/06/06 Adam change
1st 360.06R02.0001
2nd 360.06R02.0011

PCB Symbol

PCB1
(G_348.0EE02.001A,U_348.0EE07.0011)

238i GPU SA
Part Number Manufacture (Gerber Out)
348.0EE02.00SA HANNSTAR
348.0EE04.00SA GLOBALBRAN

238i GPU SA EM370

Part NumberManufacture (Gerber Out)
348.0EE09.00SAHANNSTAR (Yes)
348.0EE10.00SAGLOBALBRAN (Yes)

238i GPU SB
Part Number Manufacture (Gerber Out)
348.0EE02.00SB HANNSTAR
348.0EE04.00SB GLOBALBRAN

238i GPU SB EM370

Part NumberManufacture (Gerber Out)
348.0EE09.00SB HANNSTAR (Yes)
348.0EE10.00SB GLOBALBRAN (Yes)

GSKT1
Cable clips
(G_342.06U13.0001)

2020/01/23
Add 碟机料號: 342.06U13.0001 for GPU MB

EMI

17,24,31,68,71 PLT_RST_N — PLT_RST_N — ED8901 — AZ5725-01FDR7G-GP
24 ICH_RSMRST_N — ICH_RSMRST_N — ED8902 — AZ5725-01FDR7G-GP

SA_0205

19V_DCBATOUT

Follow EMC Suggestion
Damon Wei 1A Modify 20180109

5V_S5

5V_S0

Follow EMC Suggestion
Damon Wei 1A Modify 20180109

24,31 PLTRST_LAN_N — ED8903 — AZ5725-01FDR7G-GP

3D3V_S5 — C8901 C8902 C8903 — SCD1U25V2KX-GP — 3D3V_S0
3D3V_S0 — C8906 C8907 C8908 — SCD1U25V2KX-GP
1D8V_S5 — C8904 C8905 — SCD1U25V2KX-GP — 3D3V_S0
1D8V_S5 — C8909 C8910 C8911 — SCD1U25V2KX-GP

2020/02/18
Add cross moat cap

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS (RF/EMI)
Size: C | Document Number: Delphi_TGL-U | Rev: -1
Date: Wednesday, September 16, 2020 | Sheet 89 of 106

WISTRON REFERENCE ONLY

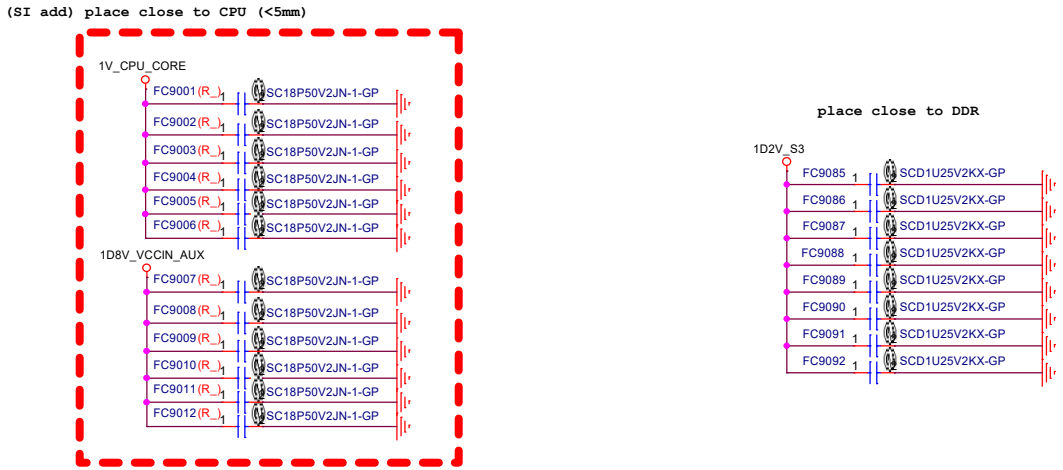

Table 9-1. VCCIN and VCCIN_AUX Decoupling Capacitors

	Cap. Placement	Capacitance
VCCIN	<= 5mm from SoC	6x15 pF (0201) or 6x12 pF (0402)
VCCIN_AUX	<= 5mm from SoC	6x15 pF (0201) or 6x12 pF (0402)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 090_INT IO (RF)
Size: A3 | Document Number: Delphi_TGL-U | Rev: -1
Date: Wednesday, September 16, 2020 | Sheet 90 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *091_INT IO (TPM)*

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 91 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *092_INT IO (Finger Printer)*

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 92 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 093_EXT IO (RSVD)

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 93 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 094_EXT IO (RSVD)

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 94 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	095_Commercial (RSVD)	
Size	Project Name: Risco215i_TGL-U	Rev: -1
Date: Wednesday, September 16, 2020	Sheet 95 of 106	

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 096_Commercial (RSVD)

Size | Project Name: Risco215i_TGL-U | Rev: -1

Date: Wednesday, September 16, 2020 | Sheet 96 of 106

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *097_Commercial (RSVD)*

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 97 of 106

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Title	*098_Commercial (RSVD)*	
Size: A	Document Number: Delphi_TGL-U	Rev: -1
Date: Wednesday, September 16, 2020	Sheet 98 of 106	

(Reserved)

WISTRON REFERENCE ONLY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *099_Debug (XDP debug)*

Size	Document Number	Rev
A	Delphi_TGL-U	-1

Date: Wednesday, September 16, 2020 Sheet 99 of 106

Conn Class	NO.	Source Priority	ME Portion			CE Portion								
			Where Use	Part No.	Qty	Vendor	Vendor P/N	Conn SPEC Center Line	Type	Pitch	S / D	Pin L	Plastic housing material	Pin
Audio Jack	1	1st	AUDS1	022.10002.0C41	1	LINGYANG	J1100D-C6DH-0002R	φ=3.6/6.0mm, H=17.0mm	Vertical		DIP	1.15	PA10T	6
		2nd		022.10002.0N41		LOTES	AJAK0069-P004A							
				3D以022.10002.0K41暫代										
Battery Connector	2	1st	BAT1	062.70001.0081	1	DEREN	40-42087-00211RHF-WH	φ/H=20/5.2mm			SMT		PA10T	2
		2nd		062.70001.0141		LOTES	AAA-BAT-063-P07_A							
CARDREADER	3	1st	CRS1	62.10051.H51	1	TAISOL	156-5001902601	H/L*W=3.8/18.75*32.1mm	Reverse		SMT		LCP	11
		2nd		Single Source										
DC Jack	4	1st	DCIN1	022.10015.0481	1	SINGATRON	2DC3012-005111F	φ=1.65/6.2mm, H=14.5mm	Vertical		DIP	1.7		3
		2nd		022.10015.00N1		LINGYANG	DC012WR-L201-016500R							
Ethernet	5	1st	RJ1	062.10005.0371	1	TCONN	23-01122-2A03-B	H=15.0mm	Vertical		SMT			8
		2nd		062.10005.0401		FOXCONN	JMP1N1Y-WBYQ9-7F							
FPC Connector	6	1st	LVDS1	020.K0368.0030	1	CVILUX	CF34302D0RE-10-NH	H/L=2.0/5.95+0.8mm	Front Lift		SMT			30
		2nd		020.K0372.0030		ACES	50692-03001-W01							
HDMI Jack	7	1st	HDMI1	062.10012.0471	1	TCONN	T13-0002-2A30	H=15.1mm	Vertical		SMT			19
		2nd		062.10012.0401		LOTES	AHDM0038-P003A							
	8	1st	HDMI2	062.10012.0471	1	TCONN	T13-0002-2A30	H=15.1mm	Vertical		SMT			19
		2nd		062.10012.0401		LOTES	AHDM0038-P003A							
DIMM	9	1st	DIMM1	062.10011.01H1	1	LOTES	ADDR0070-P009A	H=8.0mm	Reverse		SMT			260
		2nd		062.10011.01G1		FOXCONN	ASAA821-E8RB0-7H							
				062.10011.0G11		ARGOSY	D4ARN-26001-1P80							
	10	1st	DIMM2	062.10011.01C1	1	LOTES	ADDR0206-P013A	H=4.0mm	Reverse		SMT			260
		2nd		062.10011.00L1		ARGOSY	D4AR0-26001-1P40							
				062.10011.0P91		FOXCONN	ASAA821-H4RB5-7H							
M.2 M Key	11	1st	NGFFM1	062.10003.0E81	1	LOTES	APCI0164-P010H	CE/H=7.05/8.5mm	Standard		SMT			75
		2nd		062.10003.0701		BELLWETHER	80159-8581							
				062.10003.0601		FOXCONN	2E0BC21-S85BM-7H							
M.2 E Key	12	1st	NGFFE1	062.10003.0C81	1	FOXCONN	2E0BC21-S85BE-7H	CE/H=2.9/4.0mm	Standard		SMT			75
		2nd		062.10003.0E01		LOTES	APCI0163-P006H							
				062.10003.0F51		ARGOSY	NFSE0-S6701-AP85							
SPI	13	1st	SPI2	62.10076.031	1	ACES	91960-0084L							8
		2nd		CE不做建議										
SATA Connector	14	1st	SATA1	022.10019.0031	1	DEREN	40-42208-02201RHF	CE/H=3.2/4.95mm	Reverse		DIP	1.6		22
		2nd		022.10019.0021		ALLTOP	C166KK-12209-L							
Switch	15	1st	PWRBT1	062.40001.0971	1	DIP	TAFG1-13WQR	CE/H=1.7/3.3mm, H=0.85mm	Horizontal		SMT			2
		2nd		062.40004.0171		FORWARD	SFNRTMB1131T							
	16	1st	OSD1	062.40001.0971	1		TAFG1-13WQR	CE/H=1.7/3.3mm, H=0.85mm	Horizontal		SMT			2
		2nd		062.40004.0171		FORWARD	SFNRTMB1131T							
	17	1st	CMOS1	62.40089.071	1	ALPS	SKRBAJF010	H=0.55mm	Horizontal		SMT			4
		2nd		Single Source										
	18	1st	MECLR1	62.40071.001	1	ALPS	SSSS811101	CE/H=0.65/1.4mm, R to L	Horizontal		SMT			4
		2nd		062.40004.0221		FORWARD	SFSC112NAW							
USB 3.1 Gen2	19	1st	USB3R1	022.10005.0CV1	1	LINGYANG	UB1113F-L003-31AAS0R	H=14.45mm	Vertical		DIP	1.6	PA9T	9
		2nd		Single Source										
				3D以022.10005.0EL1暫代										
	20	1st	USB3R2	022.10005.0CV1	1	LINGYANG	UB1113F-L003-31AAS0R	H=14.45mm	Vertical		DIP	1.6	PA9T	9
		2nd		Single Source										
				3D以022.10005.0EL1暫代										
USB3.0	21	1st	USB3R3	022.10005.08H1	1	SINGATRON	2UB3903-055101F	H=15.5mm	Vertical		DIP	1.65	PA9T	9
		2nd		022.10005.08E1		LINGYANG	UB1113F-L040-30AAC0R							
				3D以022.10005.0FQ1暫代										
USB TYPE-C	22	1st	USCR1	062.10009.0A51	1		AUSB0316-P002A11	H=13.0mm	Vertical		SMT			24
		2nd		Single Source										
USB 2.0	23	1st	USB2R1	022.10005.0LT1	1	TCONN	18-21690-1A03-B	CE/H=4.05/6.91mm	Reverse		DIP	1.7	LCP	4
		2nd		022.10005.0K11		LINGYANG	UB1006S-C001-20AAC0R							
WTB	24	1st	CNVBD1	020.F1064.0012	1	ACES	51290-0124N-W01	H=4.3mm	Vertical	1	SMT			12
		2nd		020.F1082.0012		JWT	A1002WV0-12PS-5E							
	25	1st	CAM1	020.F1064.0008	1	ACES	51290-0084N-W01	H=4.3mm	Vertical	1	SMT			8
		2nd		Single Source										
	26	1st	SPK1	020.F1076.0004	1	ACES	87212-0044N-W01	H=4.35mm	Vertical	1	SMT			4
		2nd		020.F1077.0004		CVILUX	CI1104M1VRG-NH							
	27	1st	FANC1	020.F1209.0004	1	CVILUX	CI1504M2VR0-NH	H=5.0mm	Vertical	1.5	SMT			4
		2nd		020.F0241.0004		ACES	50288-00441-001							
	28	1st	FANC2	20.D0246.103	1	ENTERY	3801-Q03S-01R	H=4.8mm	Vertical	1.25	SMT			3
		2nd		20.F1293.003		ACES	88262-0037N-W01							
	29	1st	TOUCH1	20.F2220.005	1	ACES	50228-00571-001	H=4.3mm	Vertical	1	SMT			5
		2nd		020.F0636.0005		CVILUX	CI1105M2VR0-NH							
	30	1st	DBGH1	020.F1586.0014	1	CVILUX	CI1114M1VR0-NH	H=4.3mm	Vertical	1	SMT			14
		2nd		20.F0765.014		ACES	87212-1400N							
Stand off	31	1st	HS2	334.08002.0001	1									
		2nd												
Screw Pad	32	1st	H1,H2,H3,H4,H5,H6,H7	ZZ.SCREW.541	7									
		2nd												
LED	33	1st	LED1	83.01222.X80	1									
		2nd												

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Intel TGL-Power Up Sequence

#607872 Rev1.1 P.430

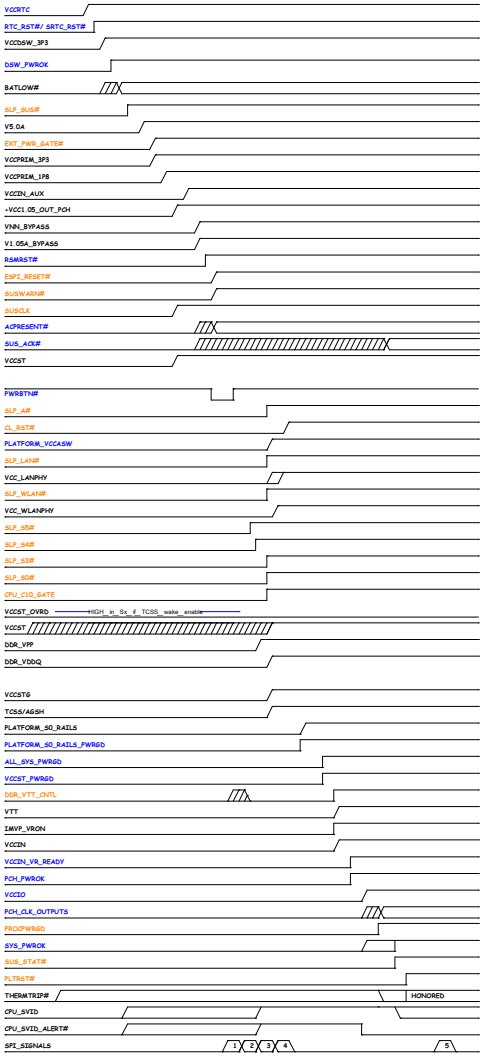


Figure 242. Premium PWROK Generation Flow Diagram

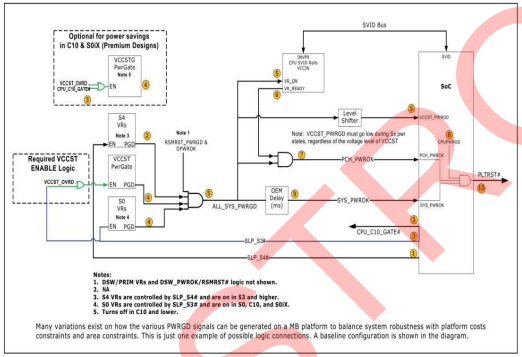
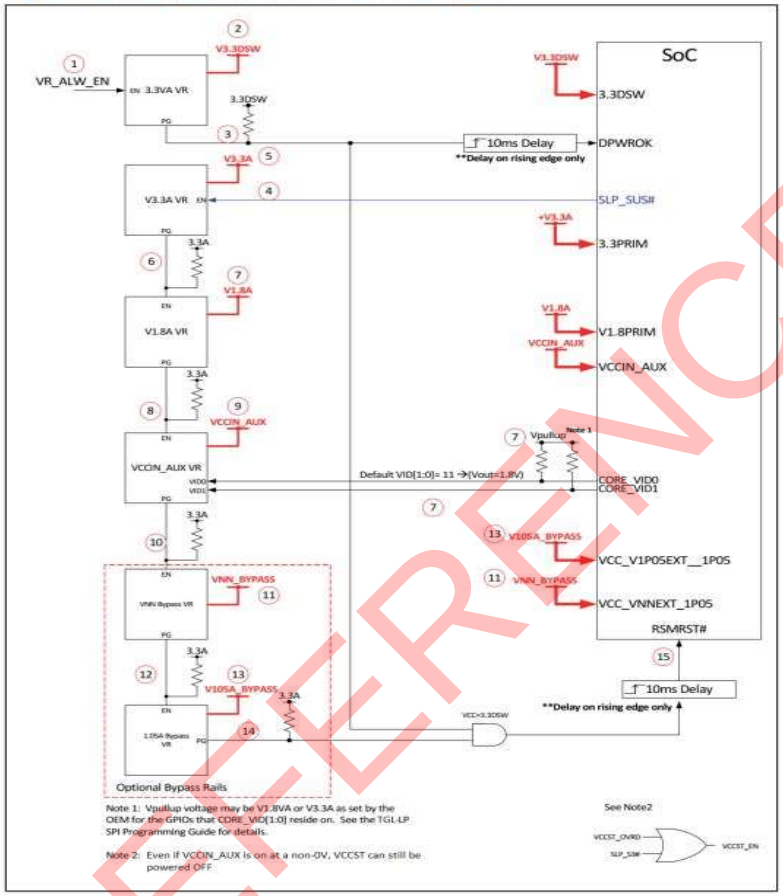


Figure 240. Tiger Lake DSx System Architecture Block Diagram



10.12.4 Power States

Table 207. System with M3 State Supported

Rails	SKUs	S0/M0 3	C102	S0ix/M-off[4]	S3/M3	S3/M -off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3[1]
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power

continued...

Rails	SKUs	S0/M0 3	C102	S0ix/M-off[4]	S3/M3	S3/M -off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3[1]
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_VNNEXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_V1P05EXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M[5]	All	ON	ON	OFF	ON[10]	OFF	ON[10]	OFF	OFF	No Power
V1.8M[5]	All	ON	ON	OFF	ON[10]	OFF	ON[10]	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST	All	ON	ON	ON	ON [13]	ON [13]	OFF[6]	OFF[5]	OFF	No Power
VCCSTG	All	ON	OFF [2]	OFF	OFF	OFF	OFF	OFF	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON[11]	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON[11]	OFF[14]	OFF[14]	OFF[14]	OFF[14]	OFF	No Power

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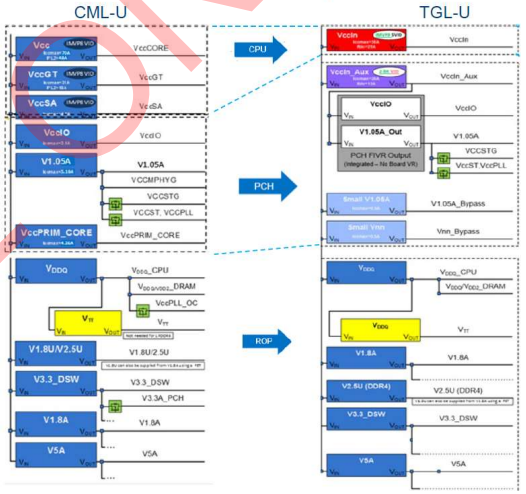
CML-U and TGL-U Power and VR Considerations (Cont..)

- TGL-U has IMVP9/FIVR implementation for both CPU and PCH power rails, whereas CML-U has IMVP8/discrete VRs for different power rails.
  - TGL-U IMVP9 Power map:
    - VCCIN: VCC_CORE and VCCGT
    - VCCIN_AUX: VCCSA, VCCIO, VNN, V1.05
  - CML-U IMVP8 Power map:
    - VCC_CORE
    - VCCGT
    - VCCSA



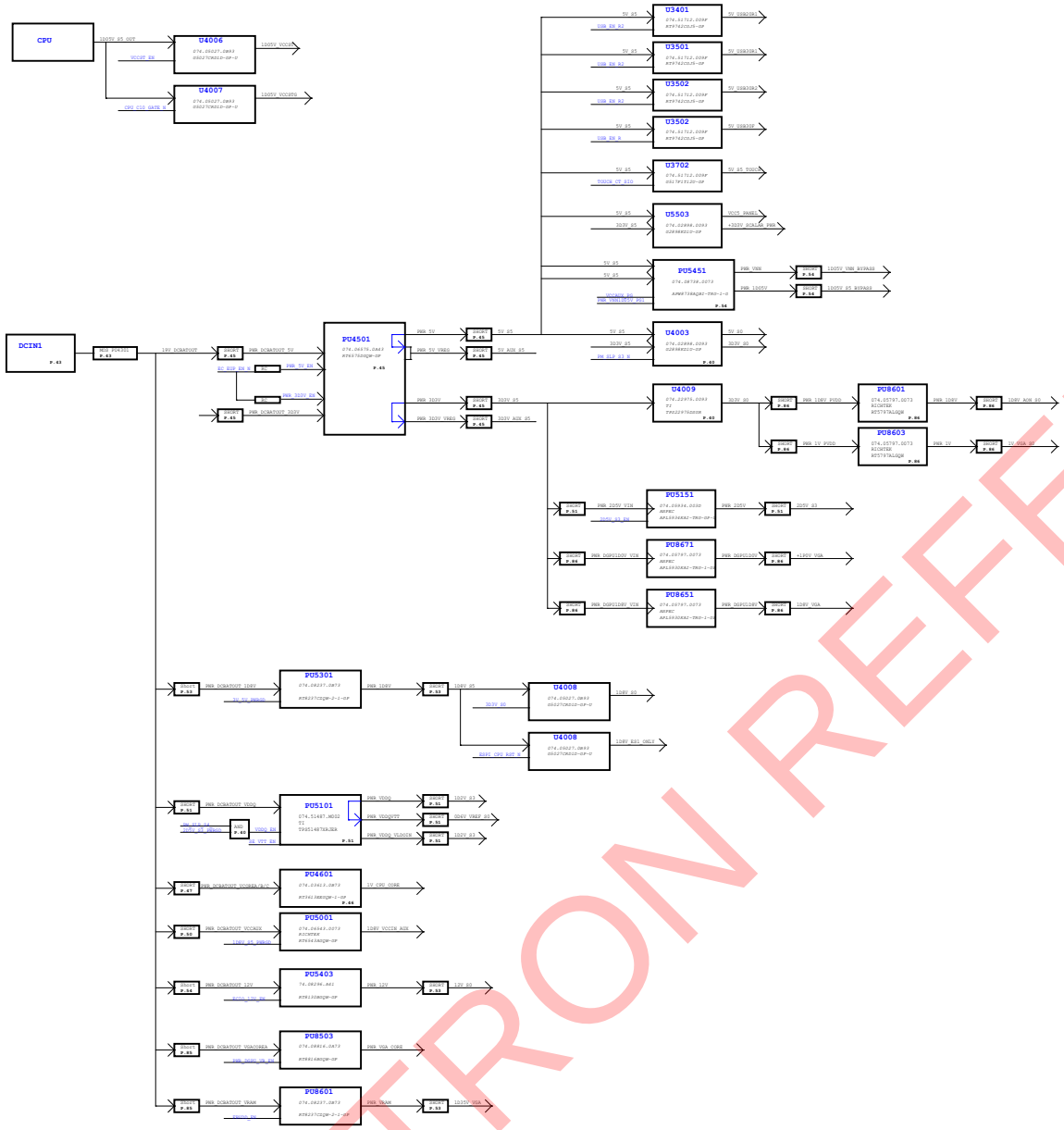


Table 10. Power Rail Descriptions for TGL U

Name	Description
VCCIN_AUX	**FIVR Input rail:** 1.8V
VCC_VNNEXT_1P05	**Used for FIVR PRIM_CORE bypass mode during Sx**: 1.05V
VCC_V1P05EXT_1P05	**Used for FIVR PCH IO bypass mode during Sx:** 1.05V
VCCA_CLKLDO_1P8	**Analog supply for internal clocks:** 1.8V
VCCPRIM1P05 _OUT_PCH	**1.05V Primary Well**: for CNVi and other internal I/O blocks.
VCCDSW_1P05	**Deep Sx Well**: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic.
VCCPRIM_1P8	**1.8V Primary Well**.
VCCPRIM_3P3	**3.3V Primary Well**.
VCCPGPPR	**Audio Power 3.3V, 1.8V, or 1.5V**. If powered at 3.3V, the 3.3V supply can come from VCCPRIM_3P3 supply. If powered at 1.8V, the 1.8V supply can come from VCCPRIM_1P8 supply.
VCCDSW_3P3	**3.3V Deep Sx Well**.
VCCRTC	**RTC Well Supply**. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. *Notes:* 1. VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations. 2. Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide (PDG) for implementation details.
VCCLDOSTD_0P85	This rail is generated internally and needs to be routed out to the motherboard for decoupling purpose.
VCC1P05 _OUT_FET	**FIVR output rail:** 1.05V, used for CPU rails VCCST/STG.
VSS	Ground

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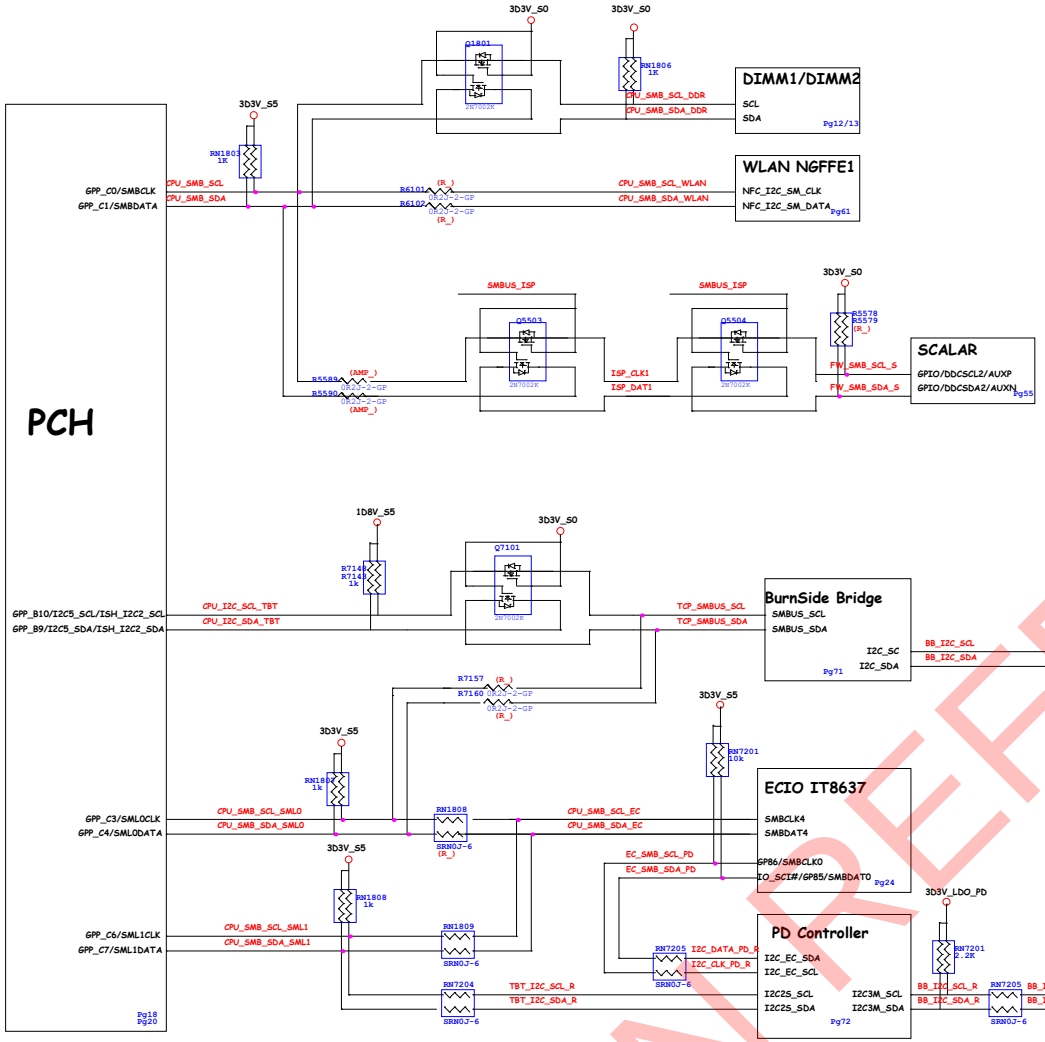
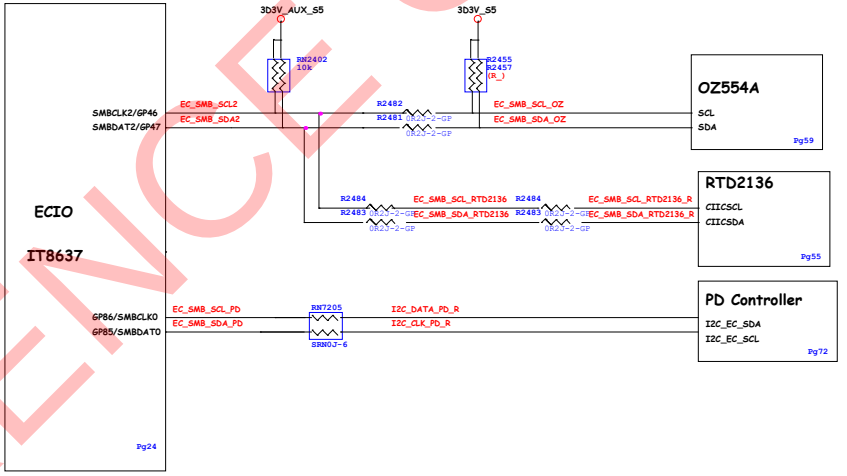
PCH SMBus Block Diagram



ECIO SMBus Block Diagram



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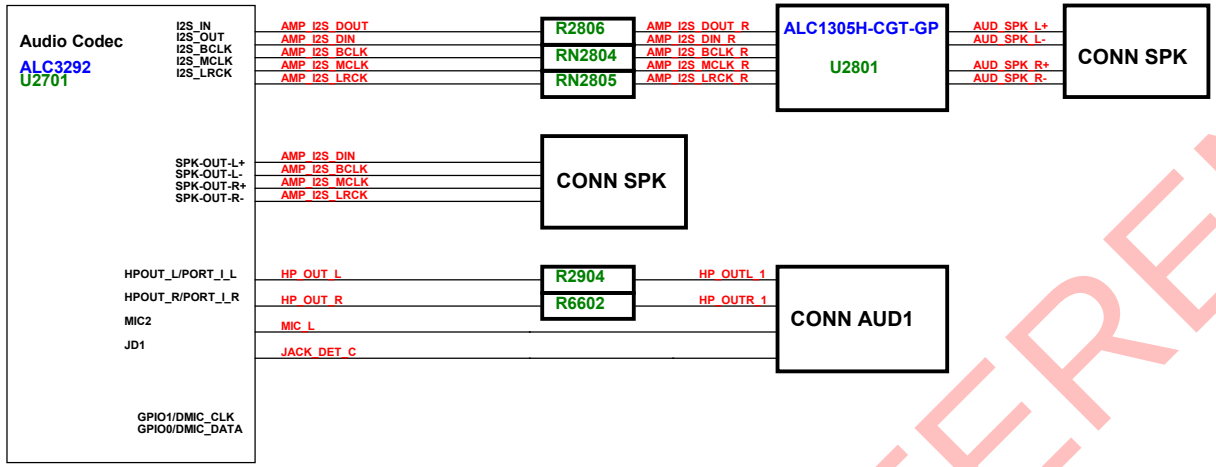
Audio Block Diagram



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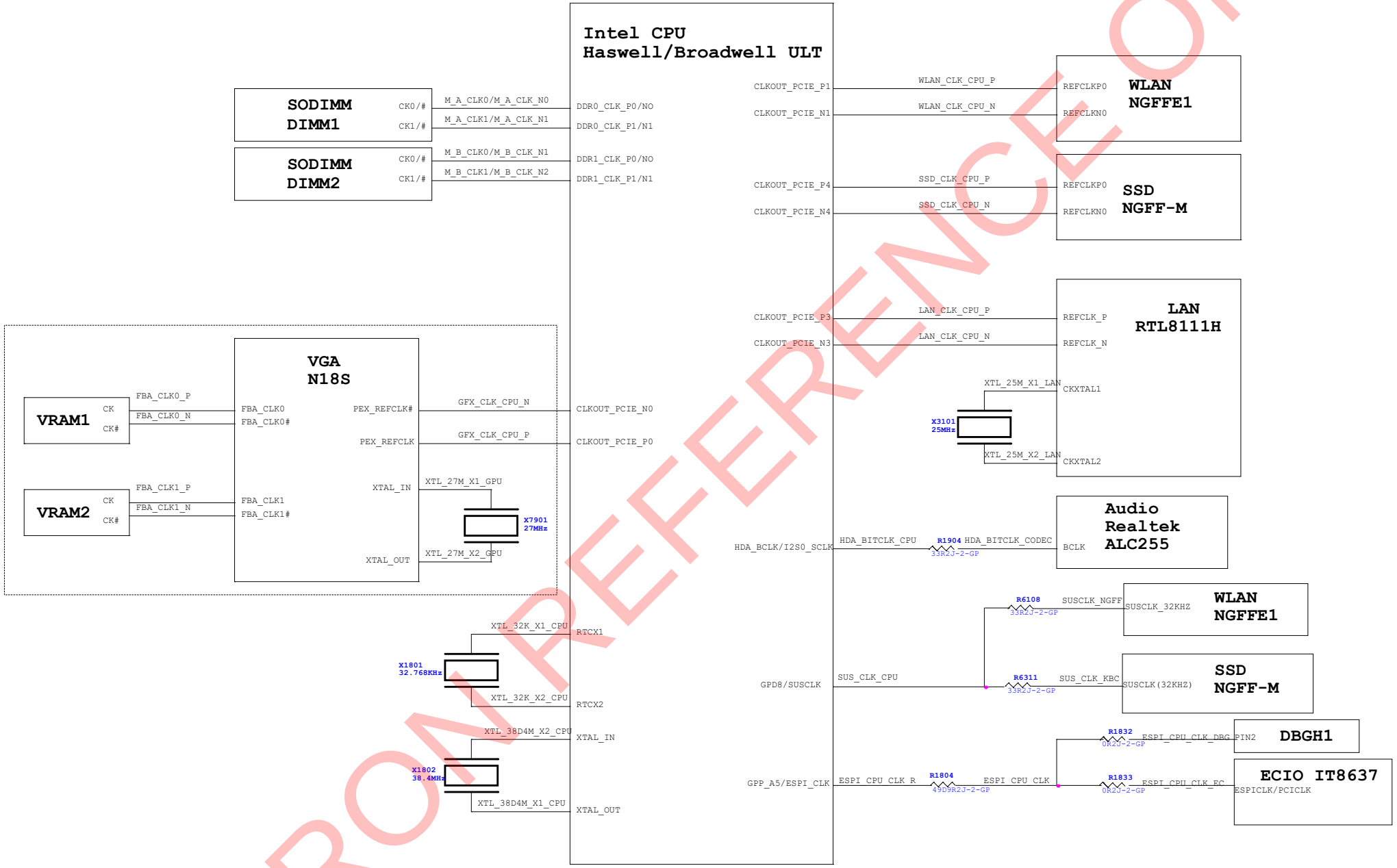
CLK Block Diagram



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